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Analysis, Design and Realization of Negative Impedance Converter Circuit with Current Feedback Operational Amplifier

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Abstract: Negative impedance converter (NIC) circuits are very interesting and beneficial building blocks with the capability of generating negative resistance, capacitance and/or inductance elements which do not exist as a singular electrical component in practice. They are commonly used for the impedance matching and parasitic element cancellation in electrically small antennas and amplifier circuits. In this study, a special kind of NIC circuit in HF band up to 30 MHz is analysed, designed and physically realised with a current feedback (CFB) operational amplifier (OPAMP) which is the core active element of the NIC circuit. The non-inverting terminal of CFB OPAMP is used for RF input signal with the elimination of DC offset voltage in the proposed NIC circuit. The negative impedance conversion capability of the circuit is theoretically proved and simulated first. This capability of CFB OPAMP to generate negative impedance is very important in high-frequency applications as they have low distortion and faster switching than that of voltage feedback (VFB) OPAMP. For the physical realizations, printed circuit board (PCB) is designed and manufactured on FR-4 dielectric material. Measurement results obtained from the realized circuit with resistive (100Ω) and capacitive (10pF) loads to be converted negatively showed that the negative impedance conversion performance of the circuit is very close to its theoretical behaviour in the lower HF frequencies generally in 3- 20 MHz band.

Index Terms: Negative Impedance Converter, Non-Foster Circuit, Matching, Current Feedback OPAMP.

1. Introduction

Negative impedance converter (NIC) circuits violate Foster's Reactance Theorem [1] because those circuits provide the negative values of resistance, capacitance and inductance. Thus, NIC circuits are also known as non-Foster circuits. In this regard, negative circuit elements generated by the NIC circuits are created in the input of a two-port system by negating its load impedance and transferring it to the input.

NIC circuits can be realized with active elements like vacuum tubes, BJTs, MOSFETs, Operational Amplifiers (OPAMP) or integrated circuit (IC) techniques in different circuit topologies and configurations. In this paper, a NIC circuit is specifically analysed, designed and physically implemented using current feedback (CFB) OPAMP to show its capability in generating negative impedance in high-frequency band between 3-30 MHz. In this manner, the differences and similarities of CFB and voltage feedback (VFB) OPAMPs are evaluated. Moreover, NIC circuit with a CFB OPAMP is designed and physically implemented that is able to generate negative resistance and capacitance. CFB OPAMPs are constructed using complementary bipolar IC technology so that they provide high-speed switching and low distortion characteristics as compared with VFB OPAMPs [29]. Therefore, implementations of CFB OPAMPs to design the NIC circuits shall provide more alternatives and flexibilities for the designers.

An important drawback of OPAMPs in terms of NIC realization is that the upper frequency limit of OPAMPs cannot exceed a few gigahertzes, and so it is lower than that of transistors [27]. Nevertheless, OPAMP based NIC circuits may be a good choice in HF, VHF and UHF band applications because of their simpler structure compared to transistorized NIC realizations. VFB OPAMPs usage are more common than CFB OPAMPs in the design of NIC circuits according to the reported studies in the literature. A Current feedback (CFB) OPAMP based NIC circuit generating negative inductance is presented in [28]. The inverting terminal of CFB OPAMP is used to realize the negative inductance conversion in the frequency range of 50-500 MHz, and a stabilization network including a resistor and an inductor are added to the NIC circuit which is reported in [28].

Non-inverting terminal of CFB OPAMP is used for RF signal input, and offset voltage elimination with a resistance in the input stage is presented in this proposed NIC circuit topology. Those are different approaches than that of the study in [28]. Simulation and test results obtained from the physical NIC circuit exhibited negative resistance and capacitance can be produced with CFB OPAMPs in the similar way as NIC circuits realized with VFB OPAMPs.

2. Literature Review

Design and realizations of NIC circuits go back to the first half of the 20th century. In the beginning, they were implemented using vacuum tubes. After the transistor era has begun, Linvill implemented the first transistorized NIC circuit [2]. He offered and described the grounded and floating types of NIC circuits with BJTs. NIC applications in the beginning were related with repeater, amplifier and filter circuits to reduce the signal loss. Nevertheless, NIC circuits can be used for the impedance matching of electrically small antennas (ESA) as well. This is because the impedance matching with NIC circuits are more advantageous than any matching with conventional passive circuits in terms of broadband matching. In this context, Sussman has given significant contributions to the matching of electrically small antennas with NIC circuits [3-6]. NIC circuit with CMOS technique using MOSFET transistors was realized by Brennan [7,8]. Moreover, some other NIC realizations with CMOS were published in [9,10]. In addition to the NIC realizations with discrete components, NICs can also be designed and produced with Monolithic Microwave Integrated Circuit (MMIC) Technology. NIC design and implementations with MMIC are reported in [12-14]. NIC technique can be applied to design integrated power amplifier circuits [15-17]. Additionally, NICs have some practical applications other than impedance matching of ESA like power electronics and wireless power transfer, which are reported in the papers [18-20]. The usage of OPAMPs is also popular in the realizations of NIC circuit [21-28]. The first NIC circuit realized with OPAMP is reported in [21] where the equivalent circuit configurations of NIC with OPAMP and the effects of non-ideal OPAMP on single OPAMP NIC realizations are discussed. In [22], some limitations of OPAMP based NIC circuits in terms of the matching capabilities of small antennas because of the parasitic components are described. Different OPAMPs based on NIC topologies are investigated and simulated [23,24]. In [25], OPAMPs finite gain and bandwidth effects on NIC performance are studied and experimentally analyzed. In [26], the effects of circuit pattern size on PCB for OPAMP based NIC circuits are analyzed with physical demonstrations showing that the smallest OPAMP packages should be selected to get the best performance. However, none of those studies has investigated the usage and effects of different OPAMP types like voltage feedback and current feedback for the NIC circuit realizations. The main objective of this study is to show NIC circuit design with CFB OPAMP in detail as in the case of voltage feedback types to benefit its high speed and low distortion features.

The paper is organized to provide theoretical analysis of the proposed NIC circuit in Section 2, practical circuit design and simulation results in Section 3, test and measurement results with the comparisons to the theoretical values in Section 4, and the conclusions in Section 5.

3. Theory

Equivalent model of the NIC circuit by using CFB OPAMP is shown in Fig. 1 below. In this circuit, V_S and I_S indicate source voltage and current respectively, Z_{in} is the input impedance of the NIC circuit, V_o is the output voltage, I_Z is the positive feedback current, I_+ and I_- are the non-inverting input current and inverting input current of CFB OPAMP, respectively. In CFB OPAMPs, there is a unity gain buffer with very low output impedance (R_0) between non-inverting and inverting inputs. T(i) is called open-loop trans-impedance gain, and it develops output voltage together with the error current i which is mirrored from the input current ($i \approx I_+ \approx I_-$). When Z_L is unconnected from the circuit, the voltage gain equation for CFB OPAMP can be written as follows [29],

$$\frac{V_0}{V_S} = \frac{1+\frac{R_2}{R_1}}{1+\frac{R_2}{T(i)}\left(1+\frac{R_0}{R_1}+\frac{R_0}{R_2}\right)} \tag{1}$$

If $R_0 << R_1$, R_2, and T(i) are very high impedance ($R_2 << T(i)$), so with the equality of $V_S = V_+ = V_-$, we can simplify the voltage gain equation in (1) as

$$\frac{V_0}{V_S} \approx 1 + \frac{R_2}{R_1} \tag{2}$$

The voltage gain equation in the case of VFB OPAMP is the same with the above derivation in (2). Hence, CFB OPAMP is similar to VFB OPAMP in terms of outer terminal relationship although their internal circuitry is different. When Z_L is placed, the Kirchhoff's Current Law for the input node of the circuit in Fig. 1 gives

$$I_Z + I_S = I_+ \tag{3}$$

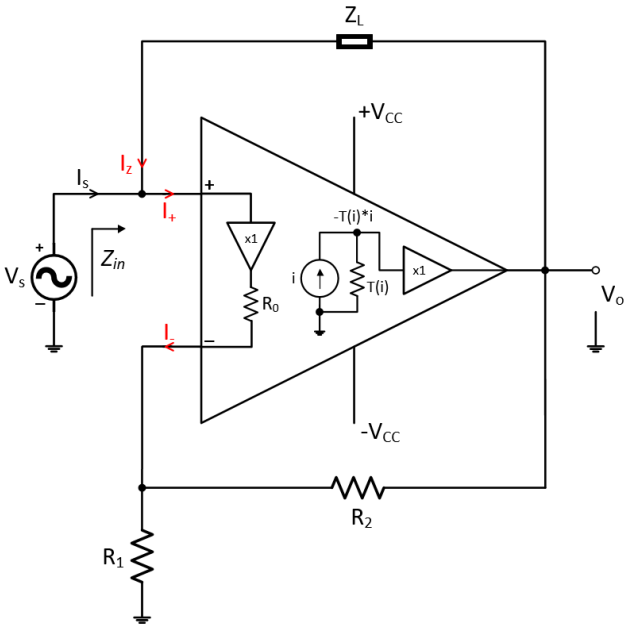

Fig.1. Equivalent model of the NIC circuit with CFB OPAMP.

As non-inverting input current is very small in CFB OPAMPs, so we have $I_S \approx -I_Z$. Non-inverting and inverting input currents for LT1210 CFB OPAMP, which is used for the physical circuit realization of this study, are given between ±2µA and ±10µA. Therefore, we can assume this approximation. The relationship between input and output voltages can also be defined by considering the positive feedback through Z_L as

$$\frac{V_0 - V_S}{Z_L} = I_Z \tag{4}$$

If we substitute V_0 in (4) with (2),

$$\frac{V_S\left(1+\frac{R_2}{R_1}\right) - V_S}{I_Z} = Z_L \tag{5}$$

Solving the equation with $I_S \approx -I_Z$, we get

$$Z_{\text{in}} = \frac{V_S}{I_S} = -Z_L \frac{R_2}{R_1} \tag{6}$$

When $R_1 = R_2$ in (6) above, "negative impedance conversion" with $Z_{in} \approx -Z_L$ is obtained from the circuit. This is the important analytical result providing the negative impedance conversion capability of the proposed NIC circuit.

4. Circuit Design and Realisation

In this study, Analog Devices LT1210 current feedback OPAMP [30] which has 35 MHz bandwidth with voltage gain (A_V) = 2 and power supply (V_{CC}) = ±15V is used. The schematics of the NIC circuit, which is designed in Altium Designer, is shown in Fig. 2 below.

In this NIC circuit above, the connectors J1, J2, J3, J4 and J5 represent positive power supply, ground connection, RF input, RF output and negative power supply connections respectively. The RF signal is applied from the non-inverting input (terminal 2) of CFB OPAMP. So, feedback resistors R1 and R2 which develop closed loop gain are connected to inverting input (terminal 1) of CFB OPAMP. The voltage gain of this circuit is 2 (≈ 3 dB) with R1 = R2 = 665Ω. The components C1-C6 are decoupling capacitors providing noise filtering. The components C7 and C8 are AC coupling capacitors to block DC voltages that are associated with the RF source voltage. The parallel resistor R4 = 330Ω is included between OPAMP input and ground to provide a path for the DC bias current. If this resistor is not used in this kind of circuit, OPAMP cannot work properly, so it cannot provide gain as expected. This is because the offset voltage in the input section of OPAMP caused by input bias currents is amplified by the closed loop DC gain of the OPAMP instead of AC signal applied in the input. The optimum value of R4 is chosen as 330Ω that is the parallel value of the feedback resistors R1 and R2 [31]. This is an important solution for this kind of NIC circuit to function correctly.The resistor R3 = 100Ω is the load that is to be converted to its negative value as a main purpose of this

circuit. Because of this positive feedback connection with resistor R3, offset voltage amplification problem occurs again in the circuit. To eliminate this problem, 5nF serial capacitor C9 is connected to R3 to block DC voltage at the output of OPAMP, so this prevents DC voltage feedback from the output to the non-inverting input of OPAMP.

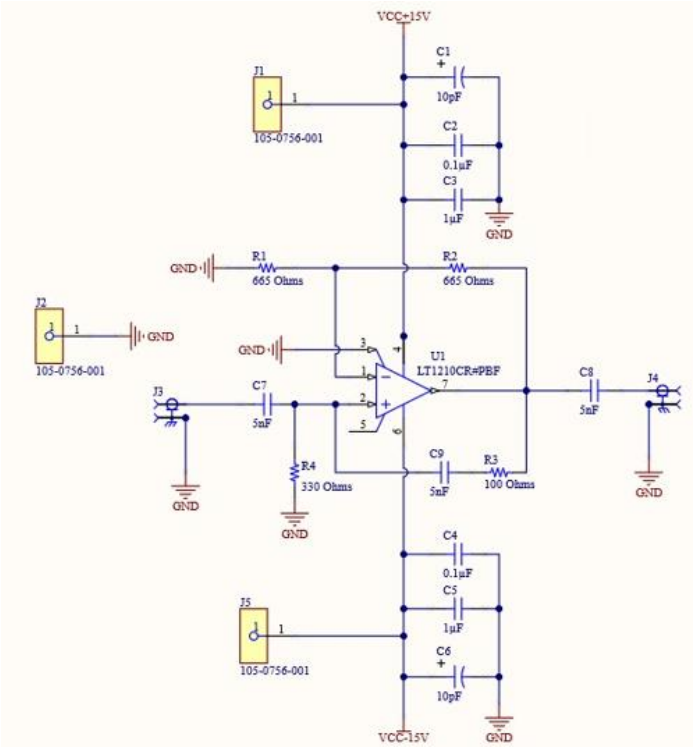

Fig.2. Schematics of NIC circuit realized with Analog Devices LT1210 CFB OPAMP.

The AC simulation of the circuit has been performed in AWR Design Environment which is shown in Fig. 3 below with no DC power supply sections. The result of the simulation with the ideal components including resistive and capacitive loads is shown in Fig. 4 and Fig. 5 below respectively. In the simulated circuit in Fig.3, the load to be converted to its negative value is the 100Ω resistor that is R3. It can be seen from the input impedance vs. frequency curve that Z_{in} is around -143Ω in 1-30 MHz frequency band for the resistive load. This is the parallel resistance value of -100Ω and R4 = 330Ω (-100Ω//330Ω) has shown in Fig. 8 below. So, the circuit is functioning in the simulation as expected.

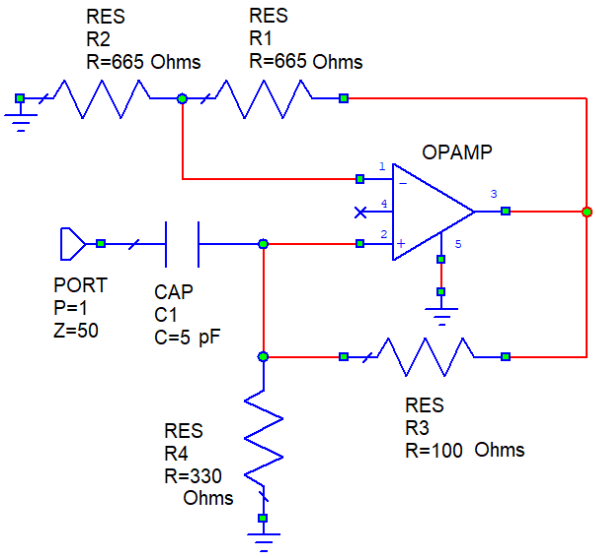

Fig.3. Simulated NIC circuit using ideal OPAMP and passive elements without DC sub-blocks in AWR Design Environment.

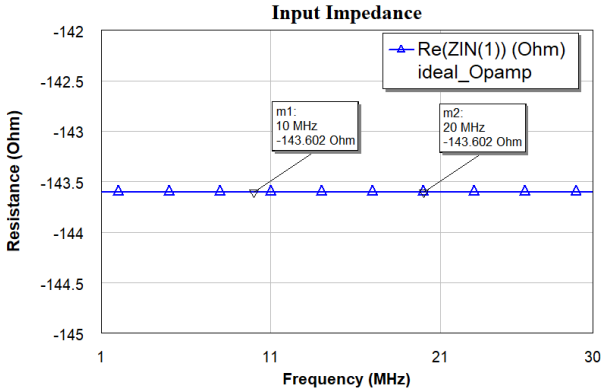

Fig.4. Simulated input impedance vs. frequency curve of the NIC circuit with resistive load.

The NIC circuit is also verified in AWR simulator with a capacitive load by replacing the 100Ω resistance with a 5pF capacitance. As we know the reactance of a capacitance is $X_C = 1/j\omega C$, so 5pF capacitor has the reactance values -3,1Ω in 10 MHz and -1,5Ω in 20 MHz. The input impedance vs frequency curve is shown in Fig. 5 below. It can be seen from the curve that the NIC circuit converts the capacitive load to its negative value by generating the reactance as +3,1Ω in 10 MHz and +1,5Ω in 20 MHz in the simulation with the ideal components.

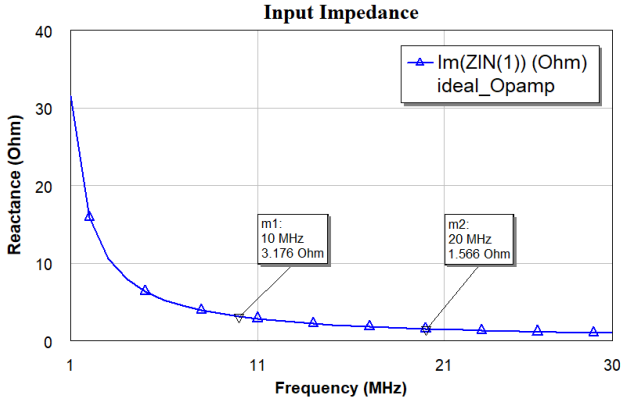

Fig.5. Simulated input impedance vs. frequency curve of the NIC circuit with capacitive load.

For the fabrication of this NIC circuit, printed circuit board (PCB) was designed in Altium Designer with FR-4 dielectric material. Total thickness of PCB is 1.4 mm with three layers. The width of RF path is 1 mm to provide 50Ω impedance in HF band on FR-4 material together with 50Ω SMA connectors in RF input and output both. The shutdown terminal (pin 3) of CFB OPAMP is connected to ground as it is not used. The compensation terminal (pin 5) is left open as it is used only for capacitive loads. The complete layout of the NIC circuit's PCB is shown in Fig. 6 below.

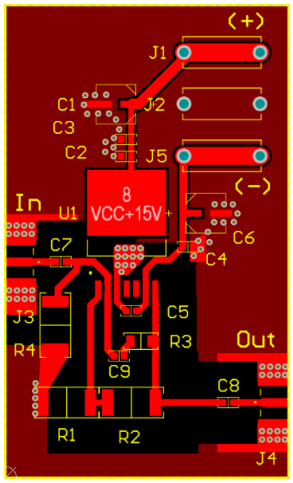

Fig.6. Layout of the fabricated PCB for the proposed NIC circuit.

5. Test and Measurements

The fabricated PCB and its test setup are shown Fig. 7 below. For the impedance, voltage and gain measurements, R&S ZNB20 Vector Network Analyzer (VNA) and Tektronix TBS2000B instruments were used. The supply current of the circuit was measured as 35 mA in both positive and negative supply paths while power supply is ±15V. The voltage gain of the circuit was also measured when there is no resistor R3 that will be converted to its negative value. It is expected that the circuit should work as a regular amplifier and provide 3dB voltage gain if R3 is removed.

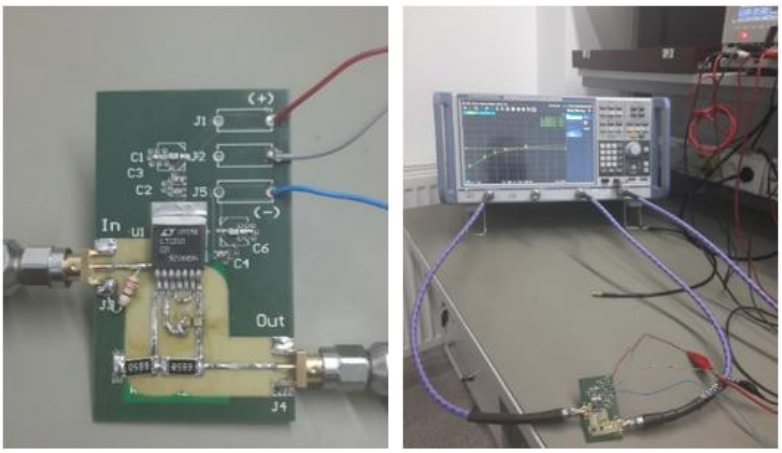

Fig.7. Fabricated PCB and test setup with VNA.

The input and output voltage waveforms, which were measured from the produced NIC circuit using an oscilloscope, are shown in Fig. 8 below, respectively. 8 MHz sine wave with 1 V peak-to-peak amplitude which is shown in yellow was applied in the input, and the sine wave with around 2V peak-to-peak amplitude was obtained in the output. It can be seen from the curves that the voltage gain of the circuit is around 3dB as R1 = R2 = 665Ω. As a result, it is verified that the circuit is functioning as expected.

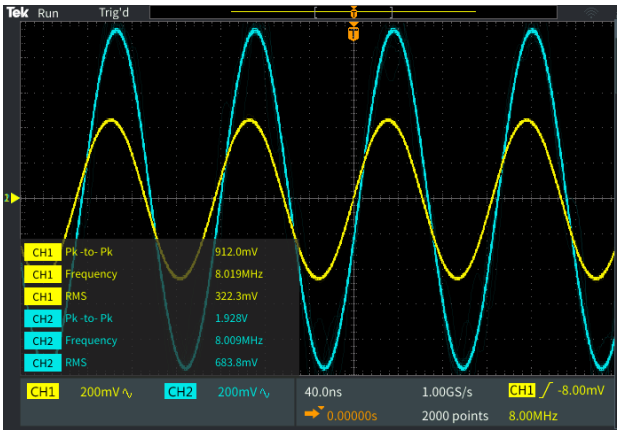

Fig.8. Signal waveforms of input and output of NIC circuit. The signal in yellow is input, the signal in turquoise is output.

For the negative impedance conversion performance of the circuit, the input impedance was measured after R3 is placed. The equivalent circuit in the input stage of NIC circuit with the addition of R4 = 330Ω is shown in Fig. 9 below. As it is seen from the NIC circuit model in Fig. 1 that it is able to produce the negative value of R3 in its input port. Because of the parallel resistor R4 for the OPAMP offset elimination, the equivalent circuit appears to be as in Fig. 9.

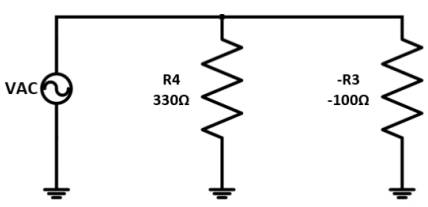

Fig.9. Equivalent circuit with the addition of resistor R4.

The equivalent resistance of R4//R3 ≈ -143Ω, so we should measure the real part of input impedance around -143Ω in the input stage of the NIC circuit. The input impedance vs frequency curves, which were measured by using two-port VNA, are shown in Fig. 10 and Fig. 11 below. Those curves in Fig. 10 and Fig. 11 below indicate the raw data directly taken from the VNA with no filtering.

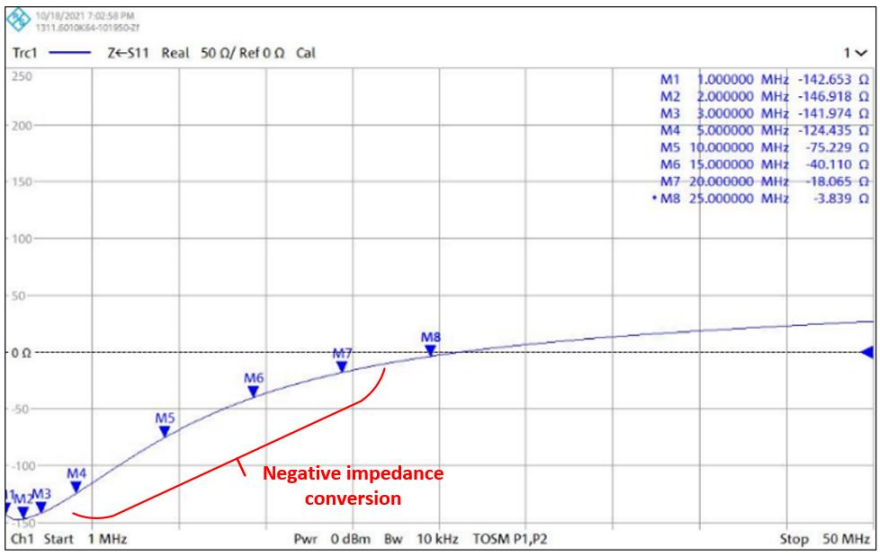

Fig.10. Input impedance of the NIC circuit with 100Ω resistive load to be converted negatively.

The negative resistance conversion performance of the circuit is better in the lower frequencies as can be seen in the chart above. The circuit provides negative resistance conversion capability up to 25 MHz. This is close to the 30 MHz bandwidth of LT1210 CFB OPAMP.

Fig. 11 shows the imaginary parts of the input impedance of the NIC circuit for the 10pF load. The circuit provides negative conversion capability for the capacitive load up to around 20 MHz. However, its negative impedance conversion performance is not as accurate and precise as in the case of resistive load especially in the upper HF band as can be seen in the curve in Fig. 11. The negative impedance conversion capability of the NIC circuit with capacitive load disappears in the frequency range above 20 MHz, and it produces unexpected reverse peak. The reasons for this deflection in the case of capacitive load are transmission line parasitic elements, PCB material inhomogeneity, non-ideal passive components used in the physical circuit, etc. Those are much more disruptive over input impedance in the case of capacitive load than that of resistive load because of the frequency-dependent parasitic effects.

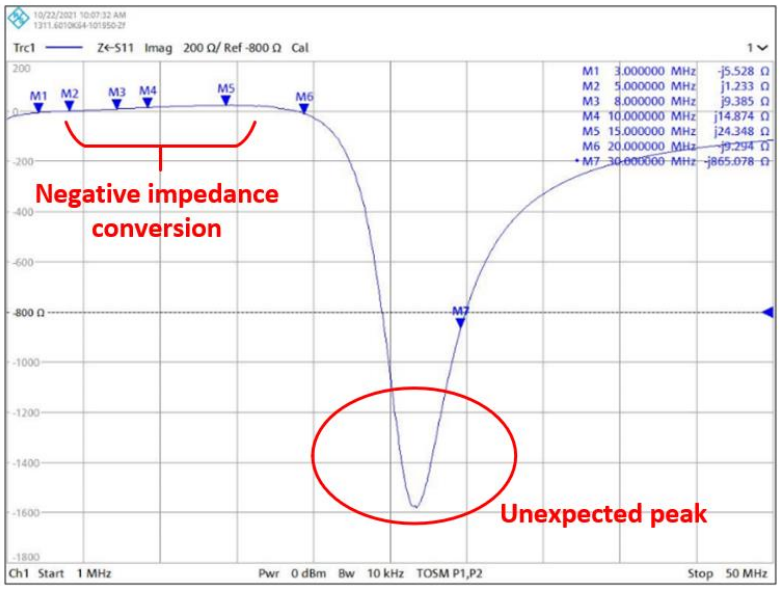

Fig.11. Input impedance of the NIC circuit with 10 pF capacitive load to be converted negatively.

6. Conclusion

In this study, we have presented the analysis, design and physical realization results of negative impedance converter circuit with CFB OPAMP. We theoretically demonstrated the capability of CFB OPAMPs for their usage in the NIC circuits. The circuit has been designed and realised physically on a PCB. Test results showed that it is able to generate negative resistance and negative capacitance by converting its load which is connected in the positive feedback of OPAMP. This is important especially for the matching circuits used in the HF band as it provides more alternatives and flexibilities for the designers in terms of CFB OPAMP usage in the design of NIC circuits. More efforts shall be performed for the CFB NIC with capacitive and inductive loads to get better negative impedance conversion results in the ongoing works.

Acknowledgments

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