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Simulation of a Ballistic SW-CNTFET with Coaxial Geometry: Numerical Approach to Determine the impact of Gate Oxide Thickness on the Performance

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***Abstract*—**Carbon Nanotube Field Effect Transistors (CNTFETs) are being proposed as candidates for next-generation integrated circuit technology replacing conventional MOSFET devices. It is a suitable nanoelectronic device which is used for high speed and low power design applications which include analog and digital circuits. In this paper, a single wall carbon nanotube field effect transistor (SW-CNTFET) with a coaxial structure in the ballistic regime has been studied and its performance parameters discussed. Numerical simulations were performed based on Natori approach. The various device metrics in consideration are drive current (I_{on}), I_{on}/I_{off} ratio, output conductance (g_d), trans-conductance (g_m), gain, carrier injection velocity, sub-threshold swing and drain induced barrier lowering (DIBL). In particular, the influences of gate oxide thickness on the short-channel effects are presented in detail. Also, the dependence of sub-threshold swing and DIBL on the gate control parameter has been discussed.

***Index Terms*—**Carrier Injection Velocity, Chirality, CNTFET, DIBL, Drive Current, Natori Approach, Short Channel Effect, Sub-threshold Swing, Tight Binding Energy, Trans-conductance.

I. Introduction

In the near future, Si-based conventional MOSFETs are expected to be replaced by CNTFETs because of downscaling limitations associated with conventional bulk MOSFETs. Scaling of channel length below 10nm in conventional MOSFETs has severely impaired their performance due to the increase of short channel effects like sub-threshold swing (SS), drain induced barrier lowering (DIBL) and threshold voltage roll-off [1]. CNTFET nanotransistors have emerged as promising alternatives to replace the existing technological limitations imposed due to channel length shortening. CNTFET offers the following advantages over bulk MOSFET: smaller size, ballistic transport of charge carriers (higher mobility), greater trans-conductance (higher gain), larger drive currents, near ideal sub-threshold slope, lower leakage current and lesser power consumption [2]. Single-walled (SW) CNT forms the channel of CNTFETs and their conductivity (semiconducting or metallic) depends upon the chirality (n, m) of the tube. The CNT channel offers a very low resistance path for the charges to reach the drain because of its superior electrical characteristics. The relation governing the nature of CNT is given by the simple equation: (n - m) = 3p. If the right-hand side of the equation is 0 or an integer multiple of 3, the tube is metallic, while for any other condition the tube is semiconducting [3].

Depending on the growth mechanism CNTFETs can have two types of geometrical structures: Planer and Vertical/Coaxial. In the coaxial structure, the CNT is completely buried inside an appropriate gate insulator, part of which is surrounded by a metal contact (gate) with suitable work function. One end of the CNT acts as the source, while the other end as the drain with a channel in between over which there is gate contact. The thickness of the gate oxide layer and its dielectric constant are very important parameters dictating the performance of CNTFETs. In fact, a very low value of the gate insulator thickness results in increased leakage current, higher power consumption and reduced device reliability [4,5]. It must be emphasized at this point that with regard to choice of the dielectric material there is a theoretical limit of gate oxide thickness, surpassing which the leakage current limits will be exceeded due to tunneling (for SiO_2 the limit is 2.3nm) [6].

In the past, researchers have demonstrated the scaling effects of gate insulator thickness on the performance of CNTFETs. It was shown that an increase in SiO_2 insulator thickness causes a decrease in drive current along with the strengthening of the short channel effects for a CNT with diameter 3nm, a threshold voltage of 0.4V, gate control of one and drains control equal to zero [7]. If the oxide thickness is reduced from 5nm to 1.5nm there is an increase in threshold voltage and the sub-threshold swing remains close to its theoretical limit of 60mV/dec [8].

In CNTFETs the use of coaxial geometry unlike planar geometry coupled with a thin insulator offers better gate controlled electrostatics. The objective of the paper is to study the effect of gate dielectric thickness on the drain characteristics, transfer characteristics, drive current, I_{on}/I_{off} ratio, trans-conductance, and gain. In addition, this paper provides a detailed insight into the dependence of short-channel effects like sub-threshold swing (SS) and drain induced barrier lowering (DIBL) on the gate dielectric thickness.

II. Analytical Model

Numerical simulation of the two-dimensional ballistic CNTFET has been done based on the Natori approach [9]. The model consists of three capacitors including drain, source and gate capacitances. The source, gate and drain potential control the mobile charge present at the top of the potential barrier through these capacitors.

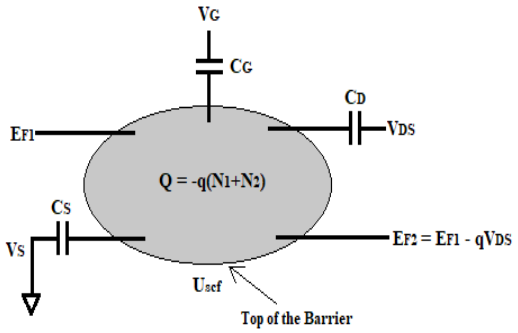

Fig.1. Two-dimensional circuit model of a CNTFET. The shaded region represents the total mobile charge. V_G, V_S, and V_{DS} represent the gate bias, source bias and drain to source bias respectively.

The electron concentration at the top of the barrier at equilibrium is:

$$N_0 = \int_{-\infty}^{+\infty} D(E) f\left(E - E_F\right) dE \tag{1}$$

where $D(E)$ is the density of states at the top of the barrier and $f(E\text{-}E_f)$ is the Fermi function at equilibrium. The function $D(E)$ takes on non-zero values for positive values of E only and is minimum at equilibrium ($E=0$). The source is always grounded in this model and when a bias voltage is applied to the drain and the gate terminals, the self-consistent potential at the top of the barrier becomes U_{scf}. The energy states at the top of the potential barrier are now occupied by two different Fermi levels (E_1 and E_2). The contribution of the source and drain in filling up these energy states can be described using the relations below:

$$N_1 = \frac{1}{2}\int_{-\infty}^{+\infty} D\left(E - U_{scf}\right) f\left(E - E_{F1}\right) dE \tag{2}$$

$$N_2 = \frac{1}{2}\int_{-\infty}^{+\infty} D\left(E - U_{scf}\right) f\left(E - E_{F2}\right) dE \tag{3}$$

where, $E_{F1} = E_F$ and $E_{F2} = (E_F\text{-}qV_{DS})$. A simplified notation of the equations (2) and (3) are as follows:

$$N_1 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_1(E) dE \tag{4}$$

$$N_2 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_2(E) dE \tag{5}$$

where,

$$f_1(E) = f(E+U_{scf}\text{-}E_{F1}) \tag{6}$$

and

$$f_2(E) = f(E+U_{scf}\text{-}E_{F2}) \tag{7}$$

The total charge concentration at the top of the barrier is the sum of N_1 and N_2 ($N=N_1+N_2$). However, in order to determine the total charge density the self-consistent potential (U_{scf}) must first be evaluated using the two-dimensional Poisson equation. The charge due to applied bias is: $\Delta N = (N_1+N_2)\text{-}N_0$. The Laplace potential at the top of the barrier ignoring the mobile charge in the channel is given by:

$$U_L = -q\left(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S\right) \tag{8}$$

Here α_G, α_D, and α_S are the gate, drain and source parameters respectively given by:

$$\alpha_G = \frac{C_G}{C_T},\ \alpha_D = \frac{C_D}{C_T} \text{ and } \alpha_S = \frac{C_S}{C_T} \tag{9}$$

where, $C_T = C_G + C_D + C_S$. For an ideal CNTFET, $\alpha_G = 1$ and $\alpha_D, \alpha_S = 0$.

The potential due to the presence of mobile charge at the top of the barrier is:

$$U_P = \frac{q^2}{C_T}\Delta N \tag{10}$$

The complete solution to the self-consistent potential (U_{scf}) can be obtained by adding the contribution of the drain and the gate in pushing down the potential energy (U_L) at the top of the barrier as well as the potential energy rise (U_P) due to the presence of mobile charge. Therefore,

$$U_{scf} = U_L + U_P = -q\left(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S\right) + \frac{q^2}{C_T}\Delta N \quad (11)$$

where $U_C = q^2/C_T$ is the charging energy. The coupled non-linear equations of (4), (5) and (11) can be solved iteratively to determine the carrier density (N) and the self-consistent potential (U_{scf}) at the top of the barrier.
The drain current can be represented as:

$$I_D = \int_{-\infty}^{+\infty} J(E) f_1(E)\, dE - \int_{-\infty}^{+\infty} J(E) f_2(E)\, dE \quad (12)$$

where $J(E)$ is the current density of states.

III. Device Structure And Input Parameters

The basic structure of the simulated SW-CNTFET having coaxial geometry is shown in Fig. 2 which has already been described in section I. In this simulation, a single wall carbon nanotube (SWCNT) acts as the channel material having a high value of doping density at the source and the drain. The following assumptions were made during the course of this investigation: contact resistance between the nanotube and metal is negligible, and transport of the charge carriers throughout the structure is ballistic (zero scatterings) in nature. In ballistic transport the mean free path of electrons is greater than the channel length; therefore the channel length does not qualify as a relevant parameter in this study.

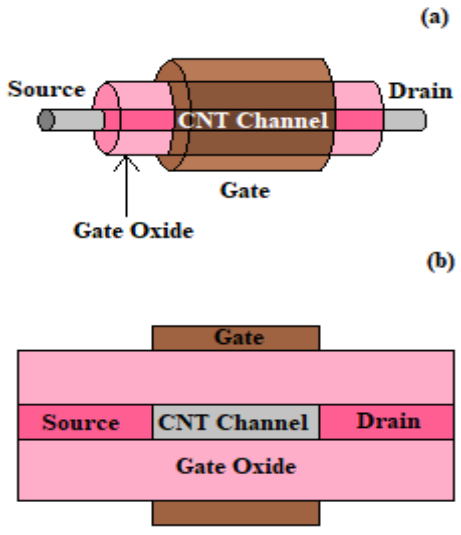

Fig.2. (a) 3-D representation of the coaxial SW-CNTFET. In practice, the source and drain ends are also buried under the gate oxide (b) simplified 2-D cross-sectional view of the SW-CNTFET coaxial structure under investigation

As discussed earlier, chirality (n, m) of the SWCNT is related to the diameter and band-gap respectively as [10]:

$$D_{swcnt}(nm) = 0.0783\sqrt{n^2 + m^2 + nm} \quad (13)$$

$$E_G(eV) = \frac{2\gamma_0 \alpha_{c-c}}{D_{swcnt}} \quad (14)$$

Where γ_0 is carbon tight bond energy, $\alpha_{c\text{-}c}$ is carbon bond length. In addition, the threshold voltage of a coaxial SW-CNTFET can be represented as [8]:

$$v_{th} = \frac{1}{\sqrt{3}} \frac{a\alpha_{c-c}}{qD_{swcnt}} \quad (15)$$

Where a is the lattice constant and q is the electronic charge. The various input parameters used in the simulation are summarised in Table 1.

Table 1. Summary of the various inputs for the simulation

Input Parameters	Values
CNT Chirality (n, m)	13,0
Tight Binding Energy (eV)	3.0
CNT Diameter (nm)	1
Energy bandgap of CNT (eV)	0.852
Gate oxide thickness (nm)	2.5, 3.0, 3.5, 4.0, 4.5, 5.0
Gate oxide material	SiO_2
Gate oxide dielectric constant	3.9
Drain Control Parameter	0.05
Gate Control Parameter	0.85
Source Control Parameter	0.0
Ambient Temperature (K)	300
Threshold Voltage (V)	0.3
Series Resistance (ohm)	0

IV. Simulation Results And Discussion

Drain characteristics and transfer characteristics are the two most important curves that help us determine the performance of FETs. From the nature of these graphs, parameters such as drive current (I_{on}), I_{on}/I_{off} ratio, trans-conductance, amplification factor (gain), drain induced barrier lowering (DIBL) and the sub-threshold swing (SS) can be extracted. In this section, the influence of gate dielectric (SiO_2) thickness on various parameters mentioned above will be discussed in detail.

A. Drain Characteristics

Drain characteristics are the variation of drain-source current with a change in drain-source voltage. Fig. 3 shows the variation of drain current for various values of gate oxide thickness. As the thickness of the dielectric layer decreases the output saturation current increases with the effect being progressively dominant. The drain conductance can be extracted from drain characteristics and is a ratio of the change in the drain to source current to the change in the drain to source voltage for a constant gate to source voltage.

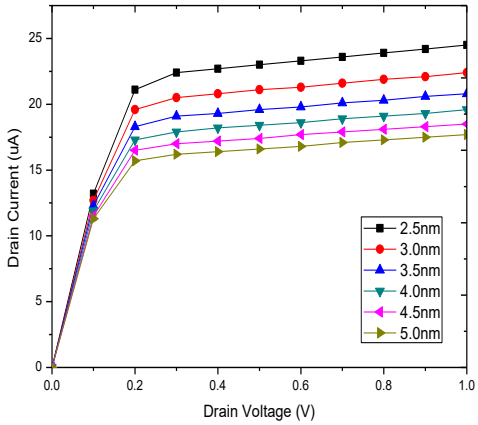

Fig.3. Drain characteristics of the coaxial SW-CNTFET for different values of SiO_2 thickness at V_{GS} = 1V

B. Transfer Characteristics

Transfer characteristics are the variation of drain-source current with the change in gate-source voltage. Fig. 4 shows the alteration in the curves of the CNTFET for different values of gate oxide thickness. The nature of the curves clearly suggests that the output current increases for decreasing gate oxide thickness enhancing the current carrying capability of the FET. From the transfer characteristics, the trans-conductance of the FET can be derived, which is the ratio of the change in the drain to source current to the change in the gate to source voltage for a fixed drain to source voltage.

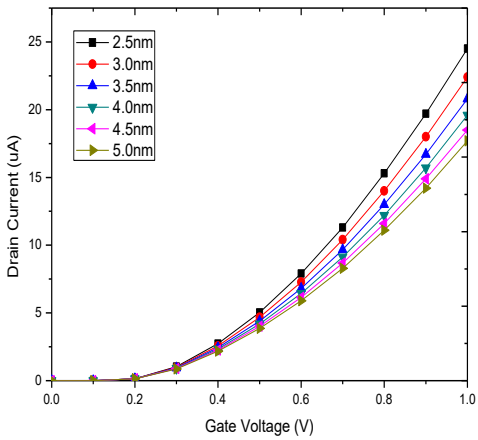

Fig.4. Transfer characteristics of the coaxial SW-CNTFET for different values of SiO_2 thickness at V_{DS} = 1V

C. Drive Current (I_{on}) and I_{on}/I_{off} ratio

One of the several advantages CNTFET offers over bulk MOSFETs is the high current drive capability. CNTFETs typically offer over three to four times the current delivering capability compared to conventional Si MOSFETs [11]. The on-current can be defined as the product of charge induced by the gate terminal and the average carrier velocity. Drive current (I_{on}) is the value of drain to source current at $V_{GS} = V_{DS}$ = 1V, while leakage current (I_{off}) is the value of drain to source current at V_{GS} = 0V and V_{DS} = 1V. The simulation results show that the extracted value of leakage current (I_{off}) remains constant at 2.556×10^{-4} μA even when the thickness of the gate oxide increases. The curves of I_{on} clearly suggest that with the increase in dielectric thickness the gate terminal loses its control over the channel, decreasing the current carrying capability of the CNTFET (Fig. 5). A similar trend is observed in the I_{on}/I_{off} curve (Fig. 6) signifying that the CNTFET on-current to off-current ratio decreases with increasing insulator thickness which is undesirable. The I_{on} and I_{on}/I_{off} values decrease by 27.64% for a mere 2.5nm increase in the thickness of the gate oxide.

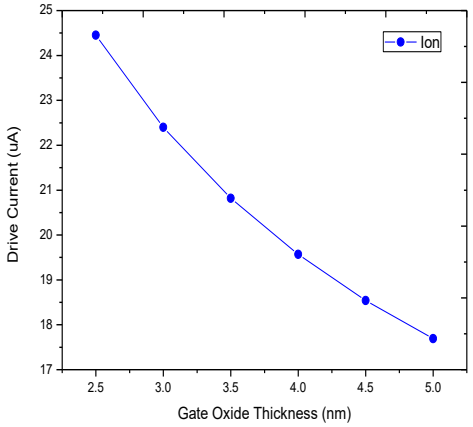

Fig.5. On current (I_{on}) of the coaxial SW-CNTFET as a function of SiO_2 thickness at V_{GS} = 1V and V_{DS} = 1V

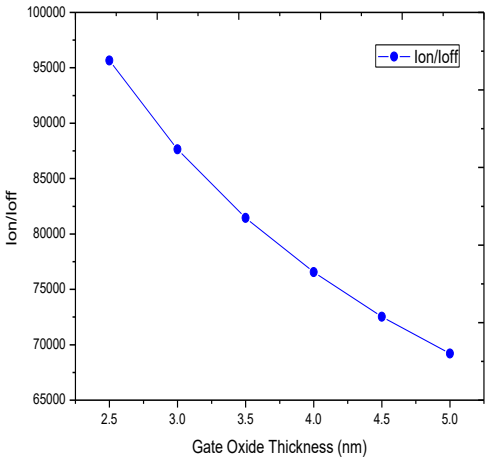

Fig.6. I_{on}/ I_{off} ratio of the coaxial SW-CNTFET as a function of SiO_2 thickness. The values of I_{off} were determined at V_{GS} = 0V and V_{DS} = 1V

D. Trans-conductance (g_m), Output Conductance (g_d), Gain and Carrier Injection Velocity

Another important parameter that characterizes the performance of a FET is the trans-conductance. For a FET this parameter should be high and is defined as the ratio of change in the drain to source current to the change in the gate to source voltage for a constant value of drain to source voltage. The value of trans-conductance of a CNTFET can be determined from the transfer characteristics. The trans-conductance of a CNTFET is typically four times higher than a conventional MOSFET [11]. It is also a good measure of the gate control over the device performance. Large value of trans-conductance suggests better control of gate terminal over the charge density in the channel. Fig. 7 shows that with the decrease in SiO_2 thickness trans-conductance value increases indicating improved gate control over the channel. For a 2.5nm decrease in thickness of the dielectric, the trans-conductance value decreases by 26.84%.

Drain conductance is a function of the drain current in the on-state and is the ratio of change in the drain to source current to the drain to source voltage at a constant gate to source voltage. The drain current decreases with the increase in the thickness of the SiO_2 dielectric (Fig. 3). Therefore, it is obvious that the output conductance decreases with increasing thickness as evident in Fig. 8.

The gain of the CNTFET is defined as the ratio of the trans-conductance to the output conductance. As far as the results of the simulation are concerned, the output conductance of the coaxial geometry SW-CNTFET varies with the thickness of the gate dielectric layer as shown in Fig. 8. The magnitude of the decrease in trans-conductance in the numerator is greater than the decrease in drain conductance at the denominator. Therefore the gain shows a decreasing trend as shown in Fig. 9. Gain is a measure of the amplification provided by the CNTFET to an input signal. Therefore, high gain is a desirable criterion in CNTFETs.

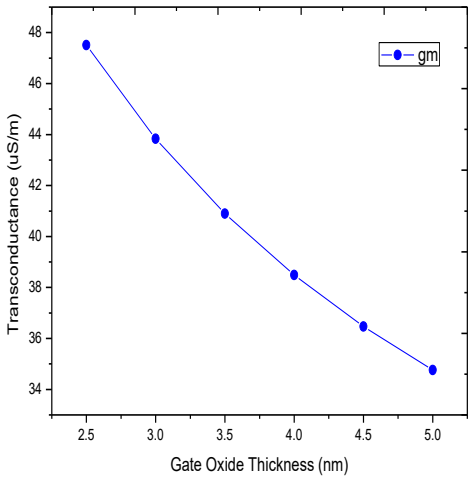

Fig.7. Trans-conductance of the coaxial SW-CNTFET for different values of SiO_2 thickness

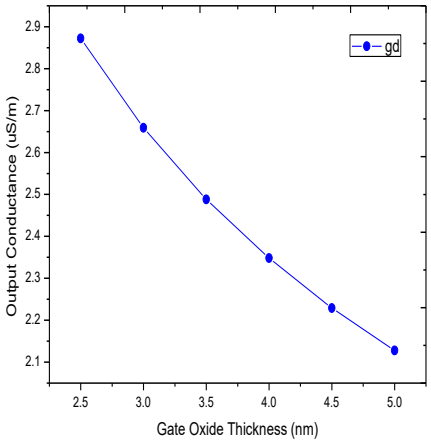

Fig.8. Drain conductance of the coaxial SW-CNTFET for different values of SiO_2 thickness

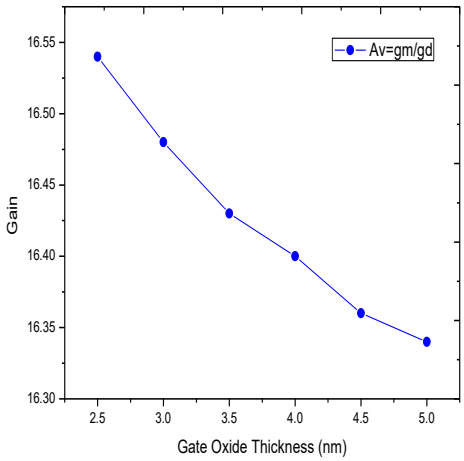

Fig.9. Gain of the coaxial SW-CNTFET for different values of SiO_2 thickness

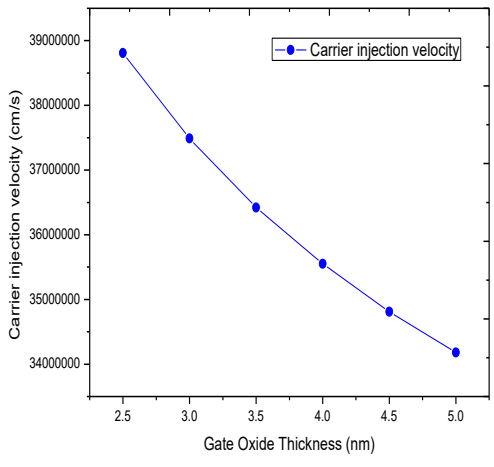

Fig.10. Carrier injection velocity of the coaxial SW-CNTFET as a function of SiO_2 thickness

Sometimes it is convenient to express the on-current of a CNTFET as the product of charge and injection velocity and is simply the average carrier velocity at the top of the barrier. The injection velocity at the highest gate bias determines the maximum on-current that a transistor can deliver [12]. Fig. 10 shows the dependence of carrier injection velocity on the dielectric thickness. The result is expected as the drain current has a direct relationship to the injection velocity. The carrier injection velocity decreases with increasing dielectric thickness, therefore the drain current follows the same trend (Fig. 3).

The results of the simulation presented thus far are in agreement with some of the studies conducted earlier on coaxial SW-CNTFETs with SiO_2 as the gate dielectric [7,8,13].

E. Short Channel effects (Sub-threshold Swing and DIBL)

Channel length shortening is responsible for the advent of two commonly observed phenomenons in nano-scale FETs: Sub-threshold swing and drain induced barrier lowering (DIBL). DIBL is a result of a reduction in the height of the potential barrier between the source and channel in the weak inversion regime because of the application of a high drain voltage. The barrier height of the charge carriers should ideally be controlled by a voltage applied at the gate. Because in a CNTFET the channel length is of the order of a few nanometers, the drain terminal is now closer to the gate playing its role in lowering the barrier height encountered by the charge carriers. As a consequence, the high electric field at the drain leads to an increase in the number of injected charge carriers increasing the off-current of the FET. Simulation result shows (Fig. 11) that the value of DIBL is weakly dependent on the gate oxide thickness and is lower than the theoretical limit of 100mV/V for a good CNTFET design [7].

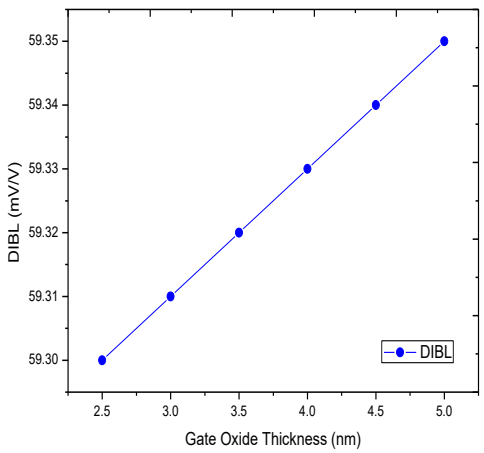

Fig.11. DIBL of the coaxial SW-CNTFET as a function of SiO_2 thickness within 100mV/decade

Sub-threshold swing is the change in the gate to source voltage required to produce a unit decade change in the drain to source current. It is a measure of the effectiveness in reducing the drain current to zero when the gate-source voltage is less than the threshold voltage. Smaller values of sub-threshold swing are indicative of lower leakage power consumption and its ideal value is 60mV/decade [14]. Also, a low value of sub-threshold swing is indicative of a fast transition between off-state (low current) to on-state (high current). Fig. 12 shows the variation of sub-threshold swing with respect to the gate oxide thickness and increases for an increase in gate dielectric thickness. Even though the value of the sub-threshold slope is best (73.61mV/decade) for the minimum gate oxide thickness of 2.5nm, it is well above the maximum permissible limit of 60mV/decade. The reason for such a high value of sub-threshold swing may possibly be attributed to the chosen value of gate control parameter (0.85).

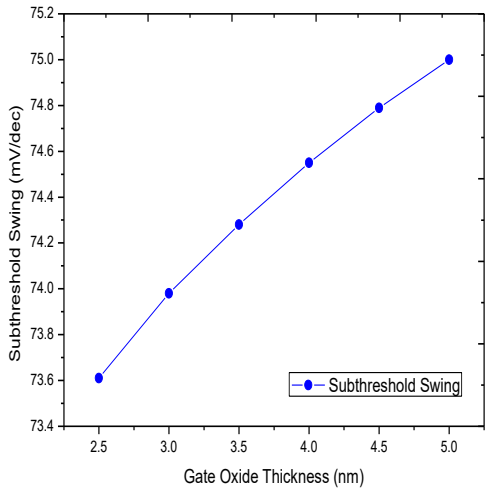

Fig.12. Sub-threshold swing of the coaxial SW-CNTFET as a function of SiO_2 thickness with values greater than 60mV/decade

The sub-threshold swing values obtained were unsatisfactory; therefore it was decided to investigate its dependence on the gate control parameter. Because the sub-threshold swing was least for SiO_2 thickness of 2.5nm, this value was chosen for a better understanding of the sub-threshold swing variation in the CNTFET for different gate control parameters. Fig. 13 shows the dependence of sub-threshold swing variation with respect to the gate control parameter. Initially, the swing decreases for lower values of gate control coefficient reaches a minimum and then gradually increases. It is obvious from the graph that in order for the sub-threshold swing to be less the gate control parameter must not be too high or too low. A smaller value of sub-threshold swing is required for providing an adequate value of I_{on}/I_{off} ratio, low threshold voltage, low power operation, and faster response. In addition, from Fig. 14 it can be observed that barrier lowering due to the electric field at the drain is also reduced when the gate control parameter is equal to unity. This means that the transition from the state of pinch-off to conduction does not happen with ease when the gate control parameter is equal to one, as a result of which leakage current is reduced.

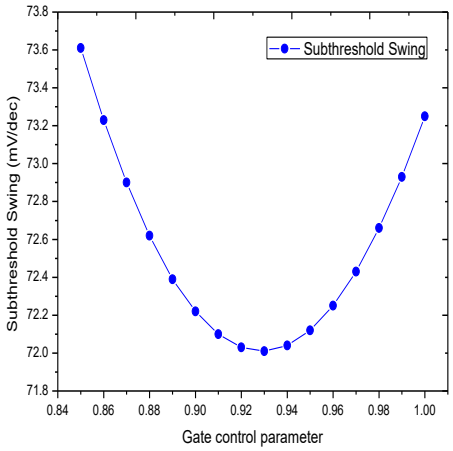

Fig.13. Sub-threshold swing of the coaxial SW-CNTFET for different values of the gate control parameter

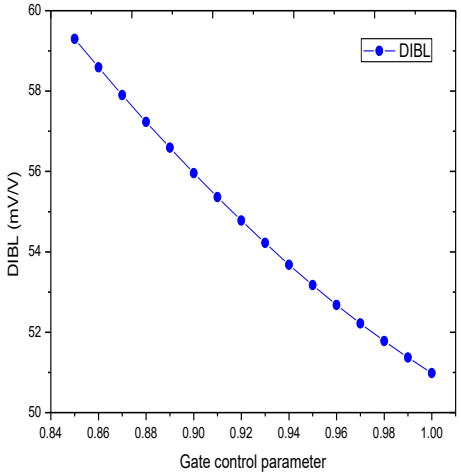

Fig.14. DIBL of the coaxial SW-CNTFET for different values of the gate control parameter

V. Conclusion

In this paper, the effects of reducing SiO_2 insulator thickness on the performance of a ballistic SW-CNTFET were presented in detail. Scaling down the gate insulator thickness improves the performance of SW-CNTFETs by increasing the drain current, driving current, on-current to off-current ratio, switching speed, trans-conductance, gain and the carrier injection velocity. At the same time, it does not have any significant impact on the leakage current and therefore power consumption is negligible. In addition, analysis of the short channel effects establishes that DIBL stays below its theoretical limit, while the sub-threshold swing approaches closer to its theoretical limit for a high value of gate control coefficient. Therefore, SW-CNTFET offers better scaling potential and faster response compared to conventional bulk MOSFETs along with lower power consumption. However, it must be noted that the gate oxide thickness should not be scaled down below a specific limit as it may lead to a rise of tunneling currents degrading the performance. In such cases, it is feasible to use a high-k dielectric instead of SiO_2 as the gate dielectric material.

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