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Enhanced Write Performance and Power Efficiency in Approximate Match CAM Using SAPON Low Power and Transmission Gate Logic

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Abstract: This project presents an architecture for approximate matching in Content Addressable Memory (CAM) systems, which are essential for search-intensive applications such as networking and genomic analysis. Traditional CAM designs often suffer from high power consumption and reduced performance. To address these challenges, this work proposes a low complexity sensing scheme that integrates transmission gate logic and a modified inverter architecture using the SAPON technique. The primary objective is to improve power efficiency and write ability in CAM systems. By incorporating the SAPON technique, the design significantly reduces power consumption, enhancing energy efficiency while maintaining high-speed functionality. Transmission gate logic improves write ability, facilitating smoother data operations, particularly in applications requiring approximate matching. The proposed design is thoroughly validated through extensive simulation using the GPDK 45nm library in Cadence Virtuoso. The results show substantial reductions in power consumption and delay, alongside improvements in performance. The optimized CAM architecture demonstrates high tolerance for mismatches, making it ideal for applications such as DNA sequencing and network routing. This CAM design provides a scalable and energy efficient solution for modern computing environments, where performance and low power consumption are critical. Overall, this design offers a reliable and energy-efficient solution for accelerating search operations in data-driven fields, positioning it as an advancement in content-addressable memory technology.

Index Terms: Content Addressable Memory, SAPON

1. Introduction

Many computer applications rely on Content-Addressable Memory (CAM), which provides quick data retrieval based on content rather than memory addresses. The perfect matching used in traditional CAM designs is computationally and resource-intensive, especially in large-scale systems. However, there is growing interest in approximation matching techniques that balancing accuracy with reduced power consumption and complexity, as a result of the growing need for scalable and effective memory solutions. This thesis explores and suggests a low-complexity sensing technique designed especially for approximation matching CAM systems in order to meet this need. It has been highlighted by the exponential expansion of data-driven applications including network routing, pattern matching, and database search. The importance of efficient memory architectures. With its capacity to facilitate associative data retrieval and conduct simultaneous searches, CAM has emerged as a viable option for speeding up these applications. However, the substantial computational power and complexity of traditional CAM designs provide difficulties, especially when dealing with big datasets and real-time processing demands.

Innovative sensing systems [1],[2] that can provide quick and energy-efficient approximation matching capabilities while reducing hardware overhead are desperately needed to address these issues. Especially in memory and sensing

applications, sense amplifiers are essential parts of contemporary integrated circuits. Their main purpose is to magnify slight voltage differences so that signals stored in memory cells or sensor elements can be reliably and accurately detected. Sense amplifiers are essential for increasing memory array readout performance, lowering access times, and boosting signal-to-noise ratios.

In Content-Addressable Memory (CAM), a sensing system is a technique for identifying and contrasting input data to be searched with data which is stored. It entails the process of sensing the contents of storage elements or memory cells and assessing whether they correspond with the supplied search data. CAMs are extensively utilized in various applications that call for fast parallel search operations between a pattern of input queries and the full data kept in unit memory [7]. In response to the growing need for similarity search in many new applications, Utilizing customized sensing schemes and other solutions (i.e., involving redundancy), a number of methods are put forth in the literature to enable approximate matching in CAMs, including comparing-intensive big data loads of work, machine learning, and pattern recognition in multiple areas of domains, including images, sequencing of DNA, and data related to biomedical.

Systems with content-addressable memory (CAM) are essential for a number of applications where quick data retrieval and search are critical. CAM execution optimization is still a major difficulty, nevertheless, especially in situations that call for approximate matching. In order to overcome this difficulty, we provide a brand-new sensing system that makes use of SAPON-modified inverter design and transmission gate logic. Our strategy seeks to improve overall performance by increasing CAM systems' writing capability and power efficiency.

2. Background

From networking to computational genomics, many compare-intensive applications require an approximation search in addition to an exact search. The new sensing method for approximate matching CAM presented in this brief [1] is intended to manage high HDs between the stored data and the query pattern. A 12-transistor +ve feedback SA and a replica mechanism are used in the suggested matchline sensing scheme (MLSS) to efficiently resolve the approximate match operation. Using 65 nm CMOS technology, the Match-line-SS was manufactured and incorporated into a 4 kB estimated CAM array. But one drawback here is high power consumption and area issues, which are compromised in our design.

TCAMs can perform table lookups deterministically and fast [2]. The main drawback, however, is how much electricity it consumes. The main source of the TCAM's power usage during match detection is MLSAs. In this study, a 20 kb TCAM with 2 MLSAs and +ve-feedback techniques is introduced. On a test chip, the proposed circuits were developed utilizing 0.18-mil CMOS technology. According to the energy measurement results, the two MLSAs have saved 52% and 44%, respectively. Here since memristors are used as storage elements consume more power which is the major disadvantage.

The consumed power in both static and dynamic leakage power has been examined in this study [3], and a novel method for reducing circuit power is presented: Stackly Arranged low Power ON transistor technology. We have implemented these strategies using a variety of CMOS logic circuits, including INVERTERs, universal gates like input NAND gate, input output NOR gate and Multiplexers, and compared their total consumption of power with the conventional reduction techniques. To comprehend the usefulness of SAPON in low-power VLSI, they looked at the suggested technique in conjunction with conventional, LECTOR and other technique like LCNT, and also considering STACK ONOFIC techniques. The results showed that Stackly Arranged low Power ON transistor utilizes lower power than typical reduction strategies. Here it is observed that more transistors are used which increase in chip area which leads to high delay .The design which we have designed addresses this disadvantage .

Systems with content-addressable memory (CAM) are essential for a number of applications where quick data retrieval and search are critical. CAM performance optimization is still a major difficulty, nevertheless, especially in situations that call for approximate matching. Therefore, a unique sensing approach that makes use of transmission gate logic and a modified inverter design using SAPON is proposed in order to meet this difficulty. This strategy seeks to improve CAM systems' write capability and power efficiency, which will raise overall performance.

3. System Design

3.1 Existing Design

Both accurate and approximate matching are possible with the HD tolerant CAM, which can withstand HDs up to 60% of the search data pattern's length. The conclusion that the matching line drop in voltage is propostionate to the HD between the searching data pattern and words of data serves as the foundation for HammingDCAM design. HDCAM approximation matching was used as a DNA classification in natural existing time designed to identify SARS-CoV-2 DNA in sample (one that contains the DNA of several different creatures) in order to assess its efficacy. Notable features of HD-CAM include its lesser area density and complexity in design, its resistance to variations in sampling duration and mistakes in sequencing of the DNA, and its capacity to withstand huge HDs with exceptional caution and precision.

Fig. 1(a) displays a m × n HD-CAM's top-level schematic view [14]. A matchline (ML) is attached to an (MLSA) for every row in the CAM. To create an n bit HammingDCAM word, a pair of lines used to search (SLs) is integrated to

each bitcell in a column, as shown in Fig. 1(b). Precharging the ML is done using the precharge (PC) transistor (MPC). A reference voltage (Vref) is used by the MLSA to determine the matchline's condition. The standard NOR-type CAM bitcell [1] is the foundation for the NOR gate type HammingDCAM bitcell, which is depicted in Fig. 1(c). Similar to a typical SRAM- 6T cell, it depends on two crossly placed coupled inverters that store data and are accessed for write and read by turning on row access via line of word WL and pre- charging or writing Line of search and Line of search to opposite values of logic. Precharge and evaluation are the two stages of the associative search process. By turning on the transistor MPC where precharge =0, the ML is precharged to VDD during the precharge

The HD-CAM cell incorporates an evaluation transistor (M4) to take charge of the line of match's discharge rate in response to the evaluation voltage level (Veval). While a traditional CAM which has exact matching operation is carried out when transistor M4 is made by a highest level of voltage, Veval = VDD, HD-CAM can accomplish approximate matching when Veval < VDD by regulating the voltage level on M4.

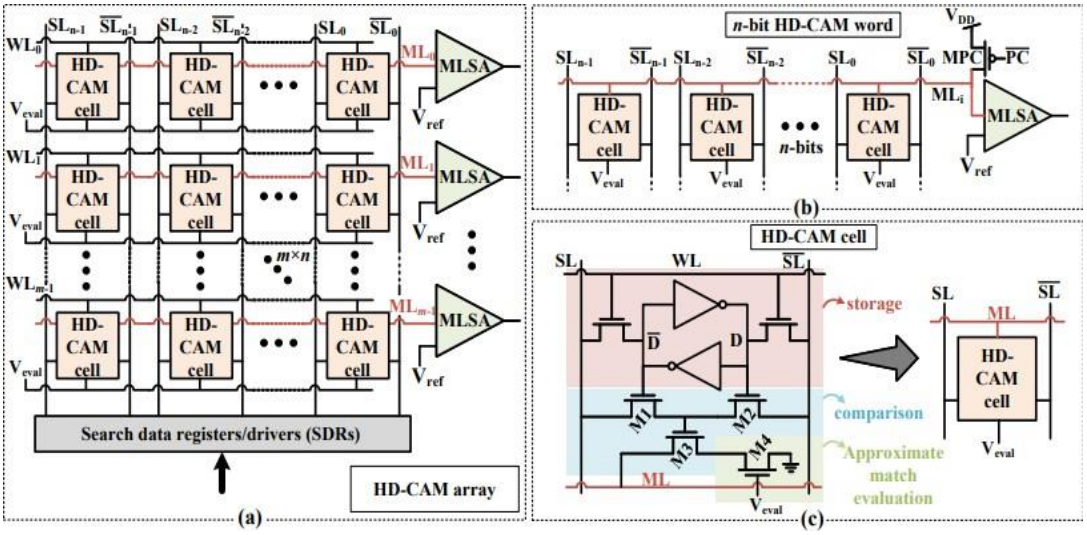

Fig. 1. Overview of the HD tolerant HammingDCAM according to on tunable match line discharge rate. (a) HammingDCAM array. (b) nbit HammingDCAM word. (c) HammingDCAM cell

The line of matching scheme of sensing (MLSS) is on a replica line-controlled +ve feedback amplifier of sensing (SA), as shown in Fig. 2 (a). The Matching Line replica line (MLRL) is made up of n parallel-connected replica transistors (Mn−1 to M0). Their source terminals are connected to the MLRL, their gate terminals are grounded, and their drained terminals are connected to VDD. An inverter (I1) and three more transistors (MN1, MN2, and MP) are part of the Matching Line SS. MP is controlled by the PC signal, as is MN2.

There is no need for a separate voltage source (or MN1) because the gate of MN1 is connected to the replica voltage (Vrep), which in the final design is the same as Veval (or VDD). However, as shown below, we allow the Vrep to be skewed independently to modify the MLRL discharge in order to assess the MLSS susceptibility to sampling time variations. The capacitance of an ML is simulated by the MLRL. The Sen signal that it produces allows for the quick detection of the positive feedback SA. The positive feedback SA's schematic is shown in detail in Fig. 2(b). Sen drives the gates of the four enable transistors (MEN1-MEN4) that make up the two cross-coupled inverters. MEN1 (MEN2) serves as the header (footer) that connects the latch to (down to) VDD (ground).

The cross-coupled inverters' output terminals are linked to the final two enable transistors, MEN3 and MEN4. Drains which are linked to the inverters that produce line of matching So and line of matching So, respectively, while the sources of the MEN3 and MEN4 devices are connected to reference voltages and line of matching, respectively. In general, the PC signal connects the MLSS activity. MLRL is charged to VDD when PC = "0," preventing the SA from sensing anything. When PreChargeis equal to "1," which permits the Matching Line RL to discharge through transistors MN1 and MN2, the comparison begins. The Sen initiates the SA sampling as soon as the Matching Line RL level of voltage falls down the I1 inverter's required threshold. The Vref and ML signals will be sent to the ends of crossingly coupled placed inverters via the MEN3 and MEN4 transistors. One terminal will rise to VDD at the greatest voltage level, while the other terminal will fall to gnd. +ve feedback amplifiers of sensing job is to contrast the Vref and ML signals. Amplifiers of sensing indicates a match (exact or approximate) when the line of matching voltage level is higher than Vref.

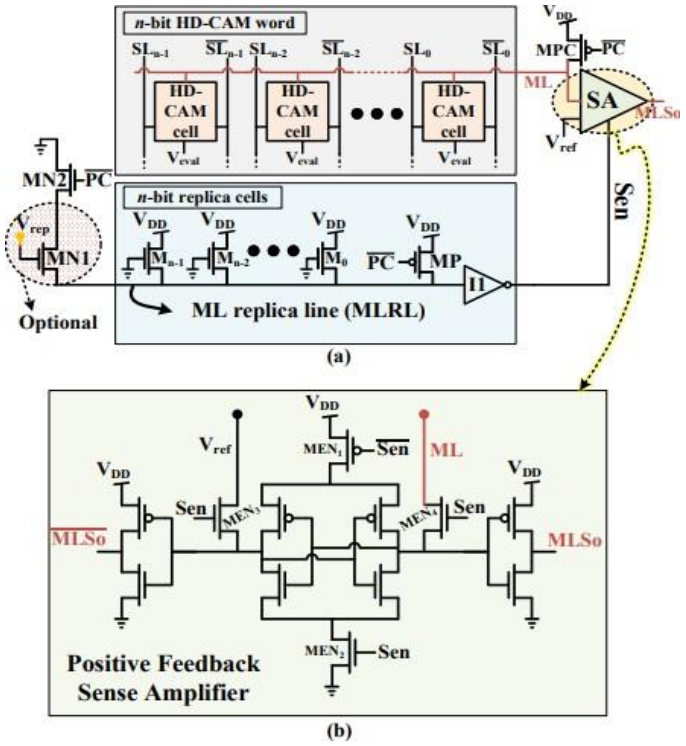

Fig. 2. Matching line scheme of sensing (MLSS) for HammingDCAM based on tunable match line discharging rate. (a) MLSS Scheme. (b) The +ve feedback sense amplifier Shematic.

The self timingly Sening signal that regulates the +ve feedback amplifier of sensing is produced by the replica row. To start the HD- CAM words sensing, theMLRL is precharged before each SA evaluation. In order to accomplish a proper procedure for searching across differences in Temperature of process voltage (PVT), this guarantees that the phase of evaluation will begin only after the precharge. The SL/SL lines and the Sen signal's delays are synchronized by the replica column. As shown in Fig. 3, this replica column, which is coupled to the Sensing line, is made up of parallel delay cells. The capacitance of the lines of search linked along the memory cell's column is represented by the delay cell.

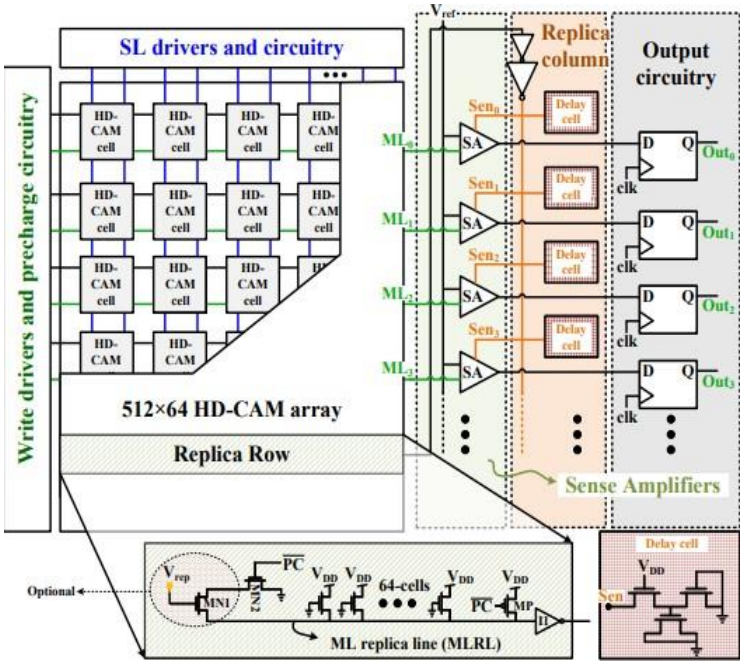

Fig. 3. HD-CAM memory array top view level architecture, matchline sensing system, and accessories.

3.2 Proposed Design

Transmission Gate Logic: Using logic levels applied externally, the transmission gate functions as a bidirectional switch made up of NMOS and PMOS transistors. Since CMOS transmission gates are switches, they can be used to switch

analog and digital signals that traverse across the entire voltage range (from 0V to VDD) in either direction. As previously mentioned, a single MOS device cannot do this. Transmission gates function similarly to voltage-controlled switches.

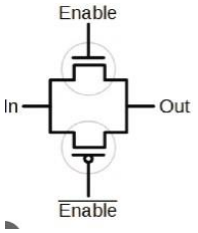

Fig. 4. Symbol of Transmission gate

Controlling leakage power, a major source of power consumption in VLSI circuits, is the core idea behind the SAPON approach. Even when transistors are supposed to be off, an undesired current flow through them causes leakage power. 2 control transistors for leakage are positioned outdoor the main logic circuit by SAPON to solve this problem. By acting as resistors, these transistors manage the leakage currents by raising the resistance between the ground and the supply voltage (Vdd).

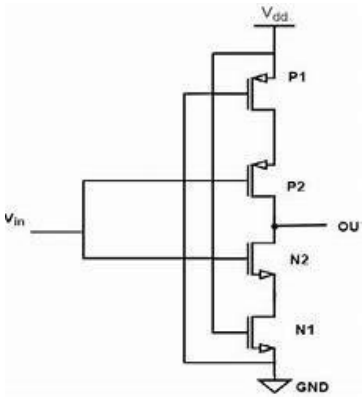

Fig. 5. Structure of SAPON

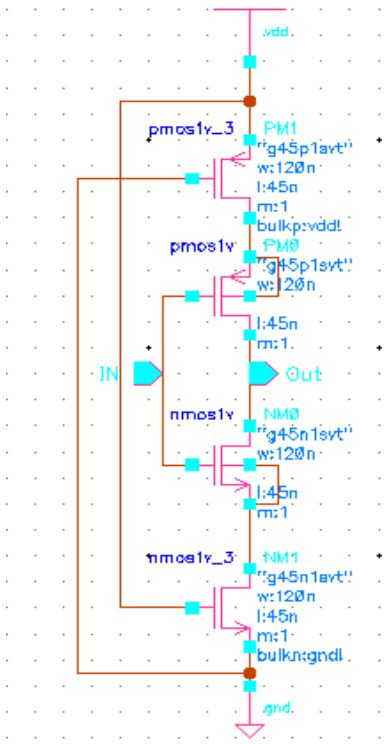

Fig. 6. Inverter Structure Modified Using SAPON

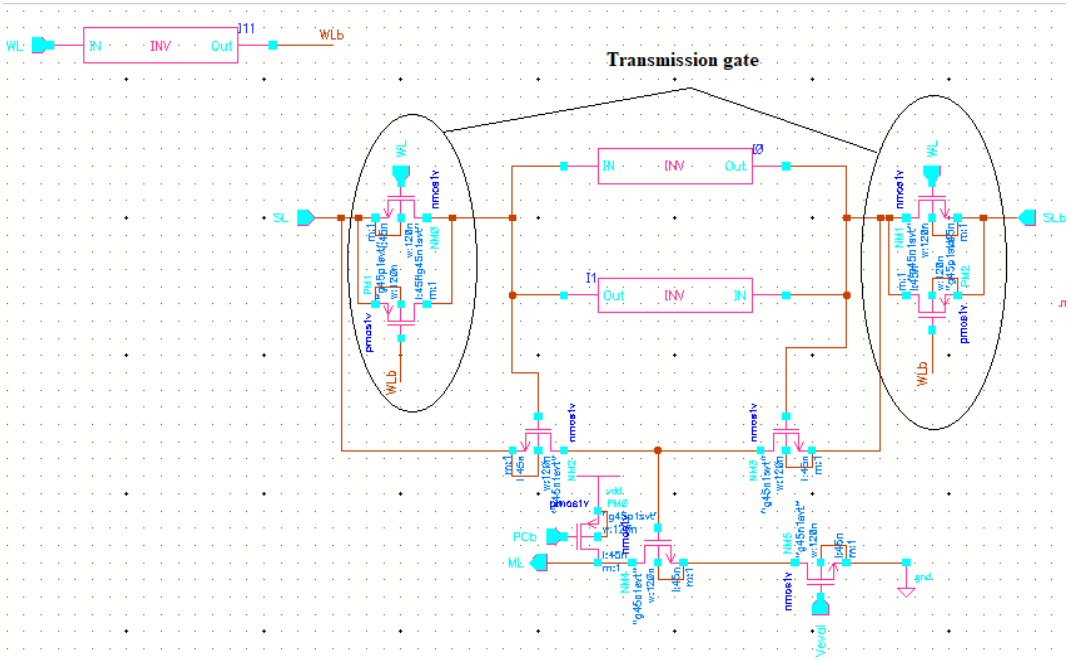

Fig. 7. Modified Architecture of CAM

Here the HD CAM structure will be modified, where the pmos transistor is connected parallelly with the nmos transistor, thus obtain equivalence resistance. A single transistor in ON state behaves has a resistor, so when to resistor are connected in parallel, the equivalence resistance decreases, hence we get faster response and overall delay is reduced. Similarly, we have used the inverter in designing the HD CAM cell. Here the inverter structure is modified using SAPON low power technology, which reduces the overall leakage current and reduces power consumption.

4. Experimental Results and Analysis

Here HD CAM cell, inverter cell, sensing amplifier, D- flip flop schematics are designed in Cadence Virtuoso using 45nm technology.

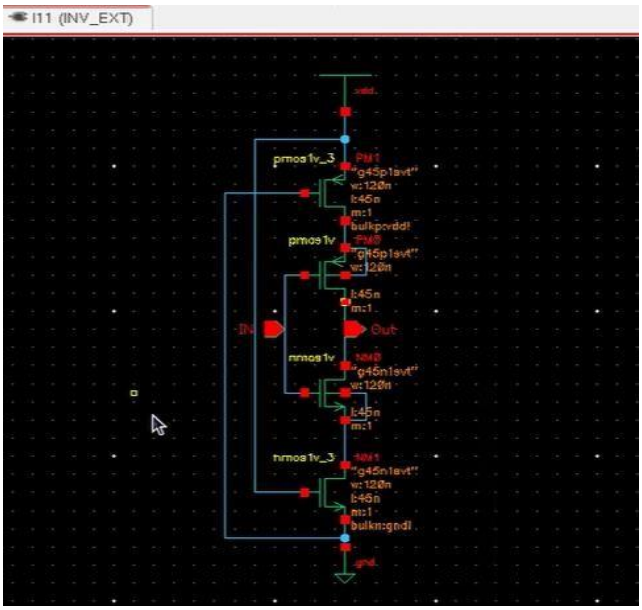

Fig. 8. Schematic of Inverter Cell with SAPON

Here in Fig. 8, the inverter cell is modified using SAPON low power technology where we use one pmos and one nmos to the existing inverter structure in order to avoid leakage current and reduce the power consumption.

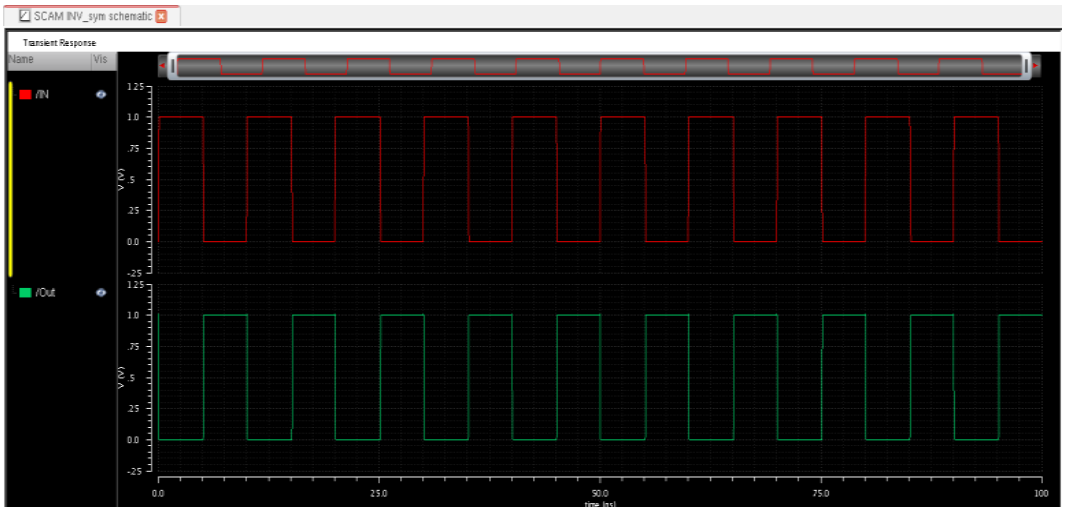

Fig. 9. Graphical results for Inverter cell with SAPON

A transient analysis graph of a CMOS inverter shows the response of the output voltage over time as the input voltage switches between high and low states. Fig. 9 Illustrates the dynamic behavior of voltage levels during the transition period.

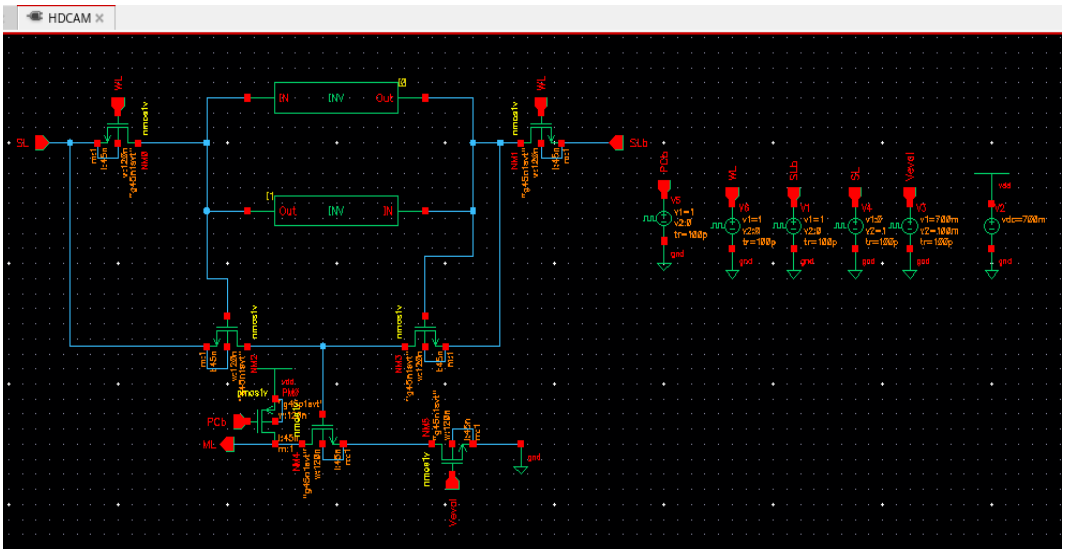

Fig. 10. Schematic of HD CAM cell

Fig. 11. Transient Analysis graph of HD CAM cell

Here in the above Fig. 11 is the Transient Analysis graph of HD CAM cell. Where the SL is the search line and WL is the four-bit word line. Here when the PCb signal and the Vevaluation signals are low, we get the exact match and when the PCb is low and Vevaluation is high we get the approximate match which can be seen along the ML line.

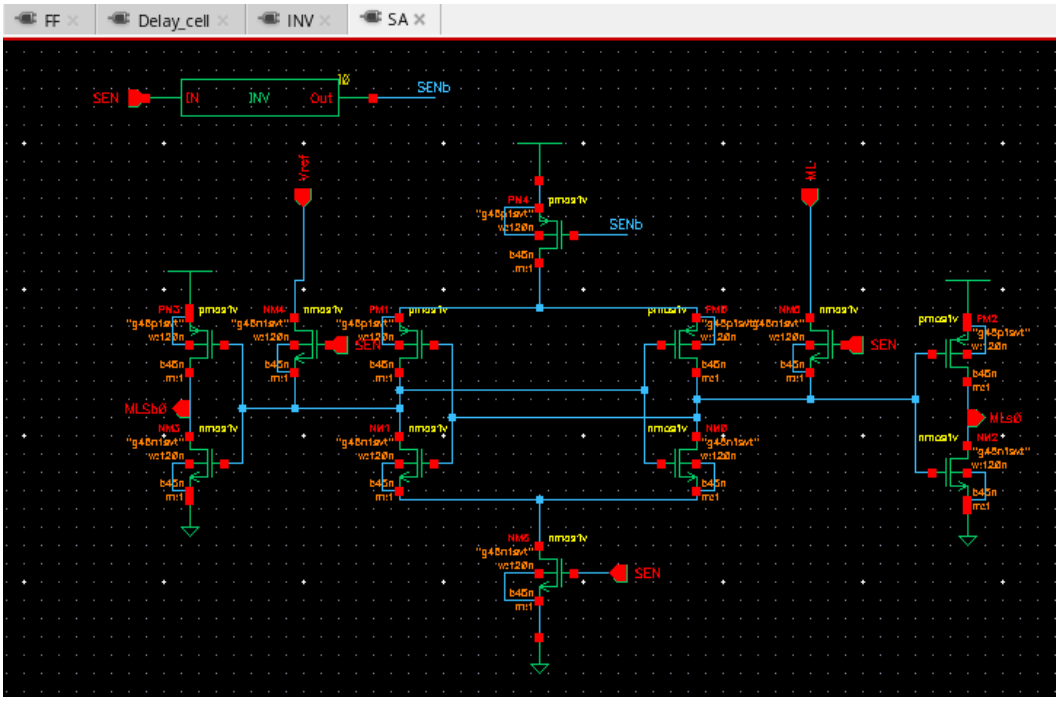

Fig. 12. Schematic of Sensing Amplifier

Sensing Amplifier which units 2 of crossly coupling inverters with 4 enabling transistors (MEN1-MEN4), where the gates are operated by Sen. MEN 2 (MEN 1) which is acting as head lead (footer) to link the latch to (towards down) VDD .Last 2 enable transistors, MEN 4 and MEN 3, are linked to the terminals at the output of the crossly coupling inverters. The sources of the MEN 4 and MEN 3devices are linked to reference voltage and line of matching, respectively, while the drains are connected to the inverters that output Matching LineSo and Matching LineSob respectively.

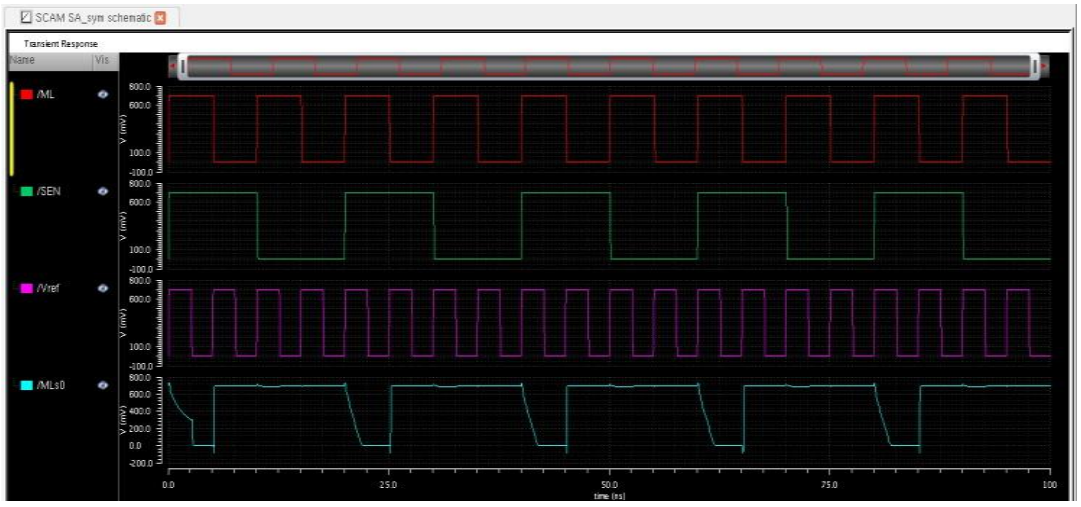

Fig. 13. Transient Analysis graph for Sensing Amplifier

Here in the transient analysis graph of sensing amplifier, the Vref signal is the input signal which is continuous input pulse which is required to activate the sensing amplifier. So whenever the sensing signal SEN is high, Vref is higher and the Line of matching will be lower, we get the MLS0 signal from the sensing amplifier which is the output. Then this MLS0 will be applied to the delay cell.

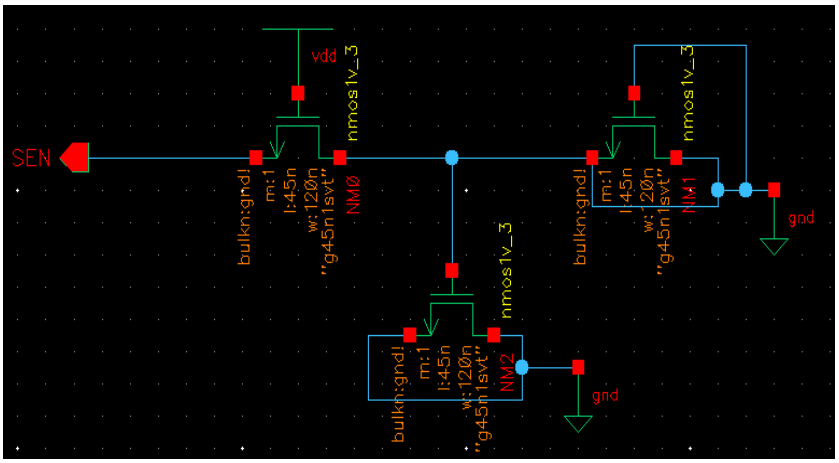

Fig. 14. Schematic of Delay Cell

This Delay cell acts as an energy storage for the output which comes from the sensing amplifier. Here both nmos are grounded and are in cutoff. Only one nmos cell will be given VDD input which will be in ON state. Hence acts as a capacitor for energy storage.

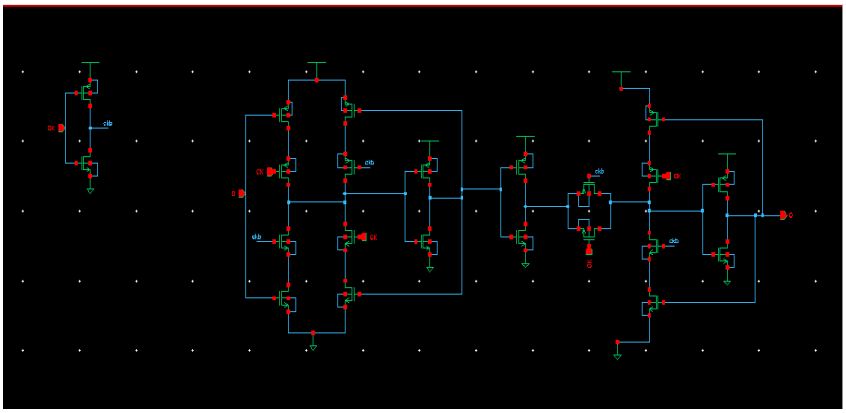

Fig. 15. Schematic of D- flip flop

A CMOS D flip-flop is a digital memory circuit that takes value of the D flip flop input at a specified clocking edge and holding it until the next clock edge. It is necessary for storage and synchronizing binary data in sequentially circuits of logic.

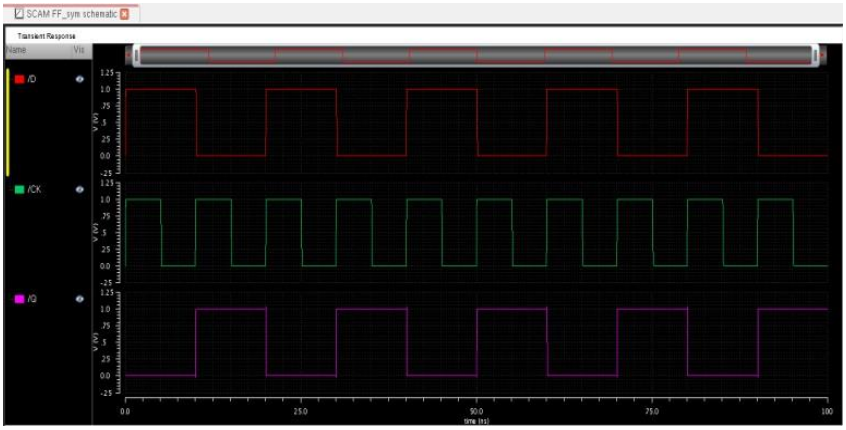

Fig. 16. Transient Analysis graph for D- flip flop

A transient analysis graph of a D flip-flop shows how the output responds to changes in the clock and data inputs over time. It helps illustrate the timing characteristics, such as setup and hold times, propagation delays, and the stability of the flip-flop during state transitions.

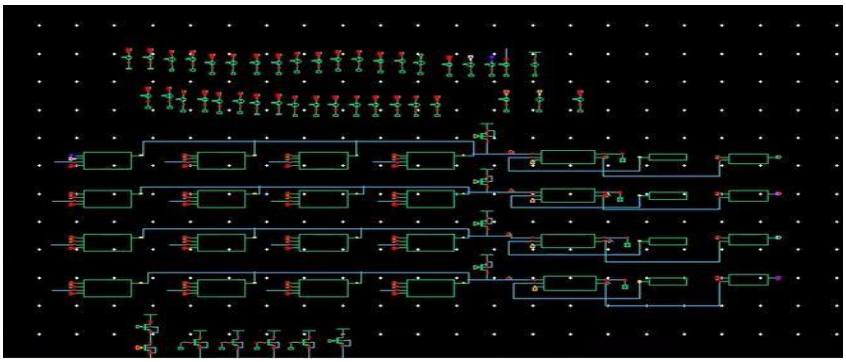

Fig. 17. Schematic of Top view level architecture of the HammingDCAM memory array with the line of matching sensing scheme and other peripherals.

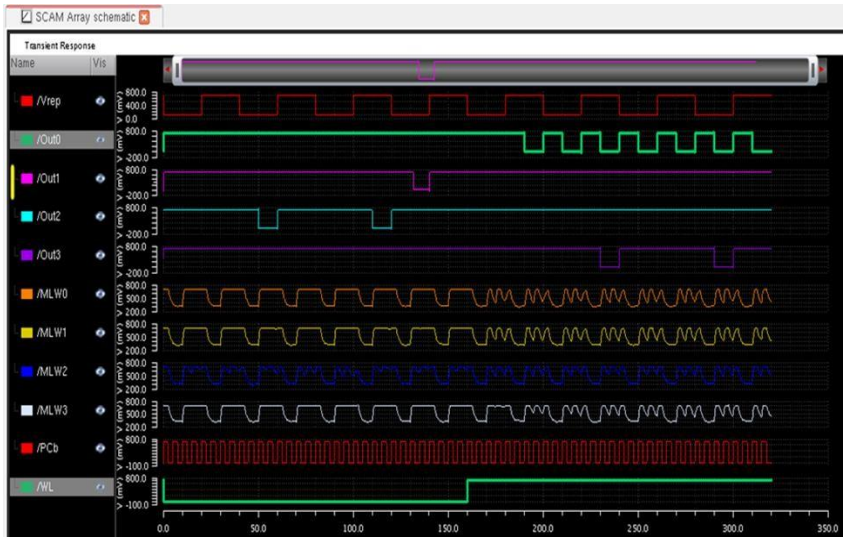

Fig.18. Transient analysis graph for Schematic of Top view level architecture of the HammingDCAM memory array.

From each HDCAM cell we have the match line ML at voltage level of 800mV. In the graph WL is completely zero and completely one, so when WL is zero it represents ON condition and WL in high state represents OFF state. As we know we are using precharge of 0 to 800mV, which in turn makes ML high at 800mV. Similarly, if all MLs are at zero voltage level, then ML word will be zero. And if any one ML is one i.e. 800mV, the ML word will be high. Here this ML is given to sensing amplifier, to get matched word MLW0. Here we will be taking different SL values, to observe different output values. So here the precharge values will remain constant. When clock is high and MLW0 is high, the output is high, again when clock is zero, output is in hold condition. when there is no change in voltage levels in MLW0, MLW1, output0 and output1 remains unchanged. hold condition. Here when there is no change in voltage levels in MLW0, MLW1. The output0 and output1 remains unchanged.

Table 1. Power and Delay Comparison table for HD CAM and HD CAM with SAPON

Design	Power	Delay	Area
HD CAM Memory Array	10.7 µW	130.5 ps	329units
HDCAM Memory Array with SAPON Low-Power	9.6 µW	120 ps	491 units

5. Conclusion

This project presents a solution to improve performance of approximate matching content- addressable memory (CAM) systems by integrating transmission gate logic and a modified inverter architecture with SAPON. The primary aim is to achieve a balance between improved write ability and power efficiency. By utilizing transmission gate logic, the design significantly improves write ability, which leads to a notable enhancement in overall memory performance. The use of SAPON in the modified inverter architecture further strengthens power efficiency, making the system more energy- efficient while maintaining its core functionalities. Extensive simulations, transient analysis, and experiments validate the success of this approach. The results demonstrate clear advancements in key performance areas for

approximate matching CAM systems, including increased speed, enhanced reliability, and reduced energy consumption. The entire design has been simulated using Cadence Virtuoso along with the GPDK 45nm technology library, make sure that the architecture is relevant and applicable to modern, scalable applications. This proposed design offers solution for environments where high-speed CAM operation is crucial, yet low power consumption is a priority. It presents a significant leap forward for memory-intensive applications in today's low-power computing platforms, providing a more energy-efficient yet high- performance memory solution. By implementing the design in an FPGA environment, evaluate its speed, power consumption, and reliability under various operating conditions. Ultimately, this prototype will serve as a crucial step in validating the design's effectiveness in modern computing scenarios.

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