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Modified Output Combining 3-Stage Doherty Power Amplifier Design for LTE Micro eNodeB

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Abstract

This paper presents a highly efficient modified output combining 3-stage Doherty Power Amplifier (DPA) design using low power LDMOS transistor for Band 40, TD-LTE Micro eNodeB. In this design, modified output combining technique has been used in the output section which meets the output power requirements of Micro eNodeB which cannot be achieved by conventional 3-stage DPA. The modified DPA design achieves 65.3% power added efficiency (PAE) at 39 dBm average output power with 20 MHz LTE signal using 15 watt LDMOS Transistor. 3-stage modified output combining technique increases the linear output power by 1.1 dB and increases the Gain flatness versus power level. The use of Digital Pre-Distortion (DPD) along with modified 3-stage DPA design achieves the linearity requirements as per the 3GPP specifications. The modified DPA combining technique has provided potential economical solution by using low power LDMOS transistor with an advantage of high efficiency.

Index Terms: DPA, Modified output combing techniques, LTE, Micro eNodeB, LDMOS.

1. Introduction

The number of subscribers using the communication services for voice and data are increasing every day. Total smartphone subscriptions reached 2.7 billion at the end of 2014 and are expected to grow to 6.1 billion in 2020 [1]. This is likely to result in an 8-fold increase in data traffic by the end of 2020 [1] and demand high network capacity with more radio resources to support high speed services like High Speed Internet (HSI), video streaming, video conferencing, file downloading, on-line gaming, Group chat etc. LTE technology (4G) is developed to meet the above projections with the help of certain inherent properties like higher order modulations and Coding (MCS), Multiple Input Multiple Output (MIMO), Beam-Forming, Carrier Aggregation, Self-Organizing Network (SON), interference mitigation features like eICIC/feICIC for

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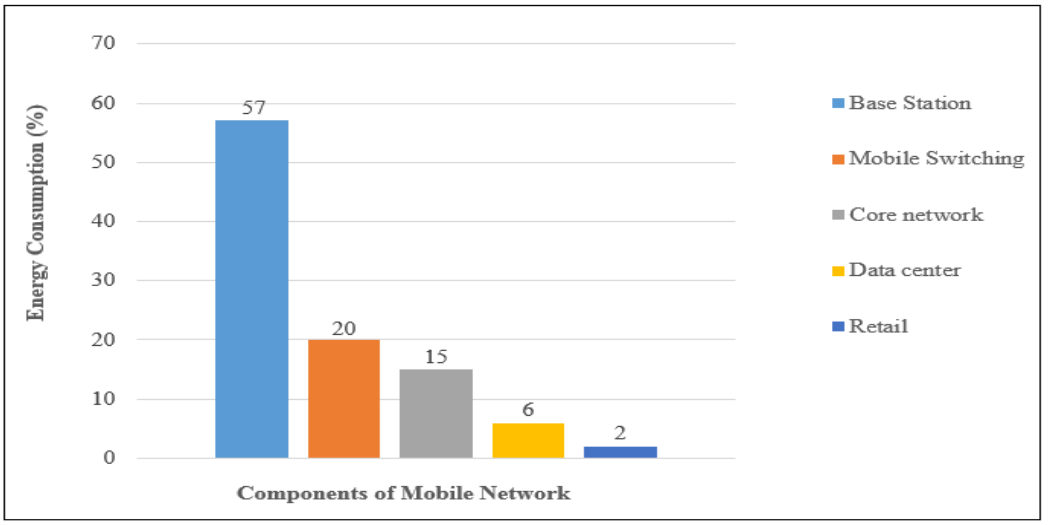
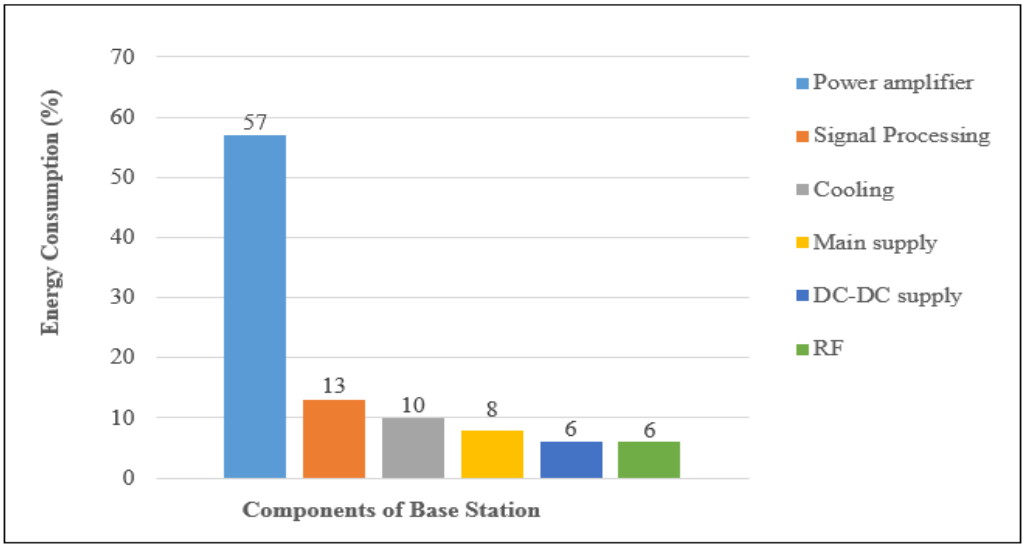
heterogeneous network and Co-ordinated Multipoint transmission and reception (CoMP) [2].

The high frequency of 2300-2400 MHz assigned for TD-LTE band 40 has more path losses compared to 800 MHz, 900 MHz and 1800 MHz band resulting into reduced coverage of LTE eNodeB. Considering one wall or two wall indoor penetration in the dense urban, urban and semi urban areas, RF coverage holes are posing a big challenge especially at higher frequency band. Micro eNodeB and small cell are considered to be a potential solution to encounter the above challenges of providing RF coverage for indoor applications and Hotspot areas. Since LTE has interference mitigation features as a part of SON algorithms [2], number of Micro sites will be deployed under the umbrella of Macro eNodeB layer. Such heterogeneous network (HetNet) with a combination of a Macro, large number of Micro sites and small cells in common geographic areas increase individual user data throughput and overall capacity of the network.

Apart from enhancing capacity and filing up the coverage holes, large number of Micro eNodeBs along with Macro eNodeBs decrease the overall energy consumptions of LTE access network significantly by shifting traffic from Macro to Micro eNodeBs. Appropriate RF Planning with Macro and Micro eNodeB instead of only Macro can save up to 46% energy consumption of access network [3]. Energy consumption can further decrease with the addition of small cell along with Micro eNodeB. Although, percentage of saving in energy consumption depends on various factors like frequency band, transmit power, antenna parameters of Macro and Micro eNodeB, interference mitigation schemes, power saving features enabled in Macro and Micro eNodeB etc., HetNet will have less energy consumption in comparison with only Macro network. Fig. 1(a) gives an overview of the energy consumption of different elements of the cellular network including 2G and 3G [4]. It indicates that base station is the most power consuming network element accounting for 57% of the total power required for telecom network. After analysing the power consumption in various base station components, it came out that the power amplifier is the most power consuming subsystem among various subsections. Fig. 1(b) represents that the power amplifier consumes more than half of the power used by a base station [4]. This proportion will remain approximately in same order for 4G LTE technology as per the initial feedback of LTE network.



(a)



(b)

Fig.1. (a) Energy Consumption for Mobile Network; (B) Energy Consumption Distribution among BTS Components

Higher order modulation increases the Peak to Average Power Ratio (PAPR), which enforces the power amplifier to be operated in the back-off region such that desired linearity is achieved as per the 3GPP standards [5]. Higher PAPR has a counter effect on the efficiency of power amplifier leading to increase in the overall energy consumption of LTE eNodeB. Further, advanced LTE features like downlink Multi User MIMO (MU-MIMO), Beam forming and Carrier aggregation (CA), require more number of transceiver chains at the eNodeBs. Since a power amplifier is required for each transmitter chain, its efficiency is a major concern for LTE and LTE Advanced.

Numerous efficiency enhancement techniques such as Envelope Elimination and Restoration (EER) (or Kahn) [6][7], Envelope Tracking (ET) [8][9], Linear Amplification using Nonlinear Components (LINC) [10], and Symmetrical and Asymmetrical Doherty have been proposed [11][12]. Although, EER and LINC are providing better performance than ET, their circuit implementation is more complex and involved tedious tuning process. Such systems are difficult to realise in the mass production. ET requires DC voltage modulator to vary the dynamic supply voltage of the bias which increases the cost and adds non-linearity due to switching of the voltage modulator [13]. Doherty design is more suitable for Macro and Micro eNodeBs due to improvement in energy efficiency up to 35% to 50% over a narrow bandwidth [14]. It can be enhanced further up to 70% using a two way Asymmetrical Doherty design with Digital Predistorted Doherty (DPD) architecture and Gallium Nitride (GaN) transistor [15][16]. GaN is a special material with high electron mobility, higher breakdown voltage and wide band gap which helps to improve the efficiency of the amplifier. Although GaN provides better efficiency, it is costlier compared to LDMOS transistor. Similar energy efficiency enhancement has been achieved through the use of crest factor reduction (CFR) and DPD with Doherty PA [17]. As per the recent studies, efficiency using LDMOS transistor for Micro eNodeB at 39 dBm average output power with 10 dB PAPR has been reported up to 60%. GaN transistor is not preferred in this design because of the economic constraint [18]. In order to achieve the best trade-off between cost and efficiency, LDMOS transistor is selected.

This paper presents a power amplifier design for 20 MHz channel bandwidth TD-LTE signal for Micro eNodeB using 3-stage Doherty design. In this design, output combining techniques have been modified which increase the linear output power and corresponding efficiency. Peculiarity of this design is that it achieves the 39 dBm output power with the use of 15 watt LDMOS power transistor, which reduces the heat dissipation, overall energy consumption and enables a potential low cost solution.

Section 2 explains the different Doherty design employed so far for increasing the efficiency of power amplifier. It also explains the advantage of the modified output combining techniques in a 3-stage Doherty power amplifier (DPA). Implementation of 3-stage Doherty design along with modified output combining circuit and corresponding impedance formulas are explained in section 3. Simulation results with single device, with 2-way Doherty, with 3-stage conventional and 3-stage with modified output combining circuit has been explained in section 4. Design presented in this paper, offers more than 65% power added efficiency for 20 MHz Downlink source for TD-LTE applications are presented in the section 4.

2. Comparison of Various Doherty Configurations

Peak to Average Power Ratio (PAPR) is approximately 10 dB or more for the higher order modulation waveforms like 16-QAM, 64-QAM and 256-QAM for OFDMA signal in LTE technology. Power amplifier (PA) is required to be operated at a back-off level of 6-12 dB from the saturation point to meet the desired linearity. While PA operates in the back-off region, it degrades the efficiency considerably. Evidently, there is a trade-off between efficiency and linearity.

In order to achieve better trade-off between linearity and efficiency, various modifications have been proposed in Doherty design including second harmonic injection [19], Symmetric Doherty design amplifiers [20], and Asymmetric Doherty design [21][22]. Second harmonic injection improves the linearity for narrow band signal but is not suitable for wideband application. In addition to this, 2-way, 3- way with symmetric design, 3-way with asymmetric design are also implemented to get the best trade-off between linearity and efficiency for the cellular base station design. Since different techniques have their pros and cons, appropriate design selection for the specific application is utmost important.

2-way symmetric and asymmetric DPA design is widely used in the commercial products due to following advantages: (i) Easy to implement. (ii) Efficiency improvement with high PAPR signal. (iii) It requires two numbers of LDMOS transistors with low power rating which will distribute the heat dissipation evenly across the PA Printed Circuit Board (PCB) instead of creating a localized thermal hot-spot. (iv) It increases the average efficiency of PA as it improves the instantaneous efficiency during the back-off operations from 0-6 dB. Basic 2-way DPA configuration consists of two amplifiers: (i) Main or Carrier amplifier biased in class AB mode and (ii) Auxiliary or Peaking amplifier biased in class C mode. Input splitter is used to split the input power between carrier and peaking amplifier. Quarter wave transmission (λ/4) line is used to combine the power at the output as shown in Fig.2.

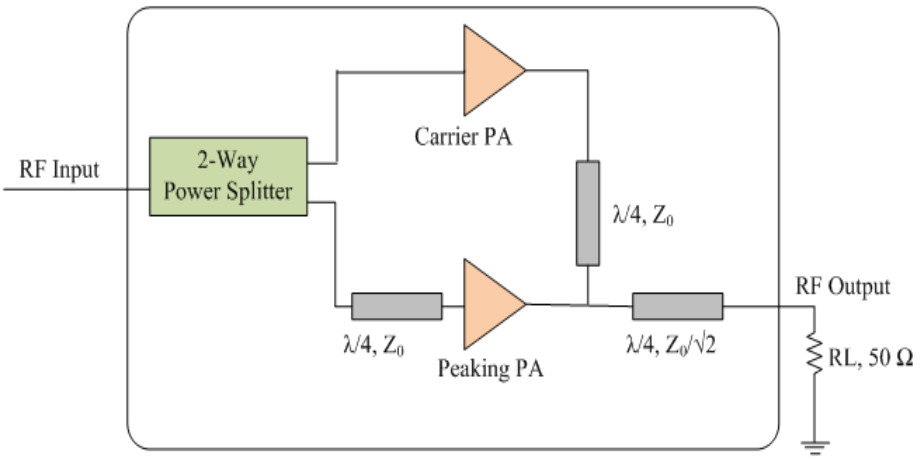


Fig.2. A basic 2-way Doherty Configuration

The detailed analysis of conventional 2-way DPA has been explained in [21]. The realization of the Doherty amplifier using solid-state devices is usually achieved by operating the carrier amplifier in class-B/AB mode and peaking amplifier in class C mode. The class-C peaking amplifier is suitable to realize a current characteristic after the breaking region when carrier amplifier will be saturated and peak amplifier will start conducting current [21]. But in this case a problem arises that the maximum amplitude of peaking current might not be reachable. This problem can be solved by using a higher power peaking amplifier [23][24] or by using uneven power divider to inject more input power to the peaking amplifier than to the main amplifier [25][26].

3-way Doherty design provides the improvement over 6 to 9 dB back-off compared to 2-way DPA. Therefore it further increases average efficiency in comparison with 2-way design. In 3-way DPA, carrier amplifier will be switched ON during low power operations. Beyond certain threshold, both peaking amplifiers will be switched on simultaneously. It will have the peak efficiency at 9.5 dB and 0 dB back-offs as shown in Fig. 3. In 3-stage DPA design, both peaking amplifiers are switched ON one by one and hence it will have peak efficiency at three different points as shown in Fig. 3 [27]. Due to more number of peak efficiency points, 3-stage DPA will provide better average efficiency in comparison of 3-way DPA. It can be designed with symmetrical and asymmetrical configurations.

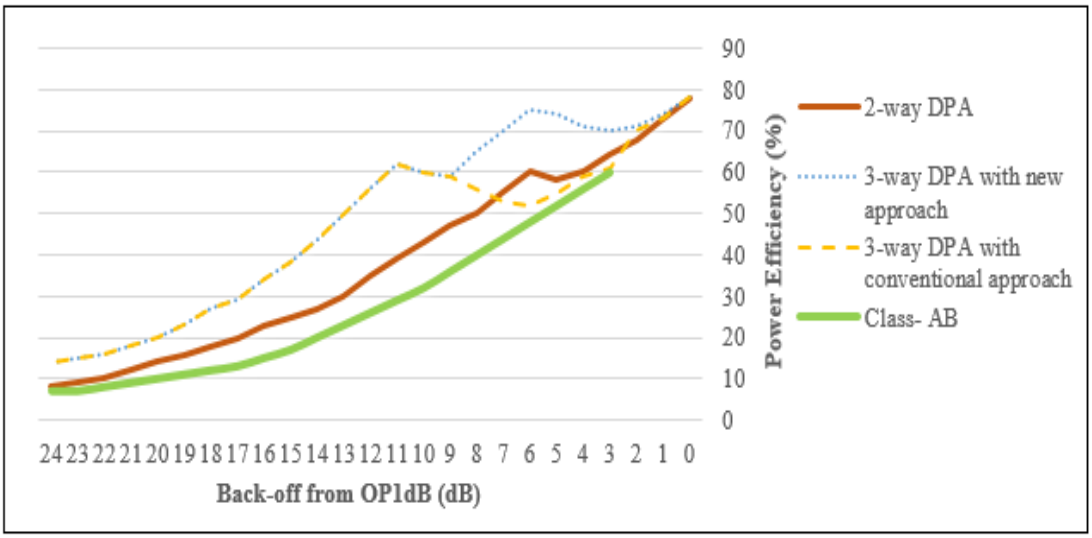


Fig.3. Power Efficiency versus Output Back-Off Level Comparison for Various DPA Configurations

Symmetrical design has the same ratio of carrier and peaking amplifier power rating while asymmetrical design will have higher power rating of peaking amplifier compared to carrier amplifier. 3-stage DPA is explained in details in following paragraph.

Fig. 4 explains the high level block diagram of 3-stage conventional DPA design [28]. Power splitter is used at the input section to divide the input power in three different branches. One branch feeds power to the main amplifier and the other two branches feed power to two peaking amplifiers. High level block diagram is common for both 3-way and 3-stage symmetrical DPA Design except the bias voltage for peak amplifier.

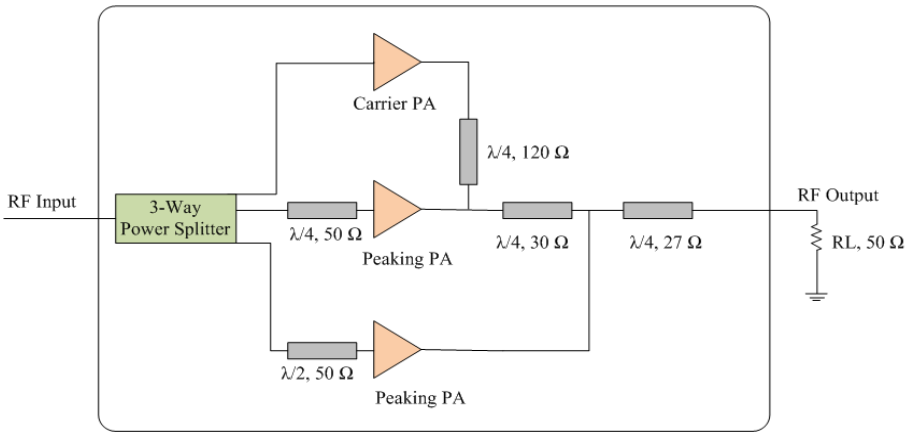


Fig.4. A Conventional 3-Stage Doherty Configuration

Efficiency increases gradually from 2-way DPA, 3-way DPA to 3-Stage DPA design. As we move from 2-way to 3-way design, switching ON/OFF of transistors increases which in-turn decreases the linearity. So far, 2-way DPA along with DPD is the most popular technology commercially used by the base station manufacturers due to optimal trade-off between efficiency, linearity, cost and practical implementation [15]. DPD algorithms have evolved over a period of time. As per recent studies, up to 25 dB improvement in Adjacent Channel Power Ratio (ACPR) has been reported by DPD algorithms [29]. It enables the use of 3-stage DPA to achieve high efficiency in practical scenario.

A typical issue associated with the conventional 3-stage DPA is that the dynamic load modulation of the carrier amplifier stops at a certain power level, leaving the Main amplifier in deep saturation and leading to significant degradation of its linear performance [27]. Moreover, it is difficult to achieve the uniform gain profile versus power level due to switching ON and OFF of three power transistors in 3-stage DPA design. It is also called as "Dividing loss". In order to achieve better flat gain profile with reference to power level, dividing loss should be compensated by high gain arising from load modulation [27]. This issue can be partially solved by using an output modified combining network as shown in Fig.5. Next section explains the theory and practical implementation of output modified combing techniques with 3-stage Doherty design.

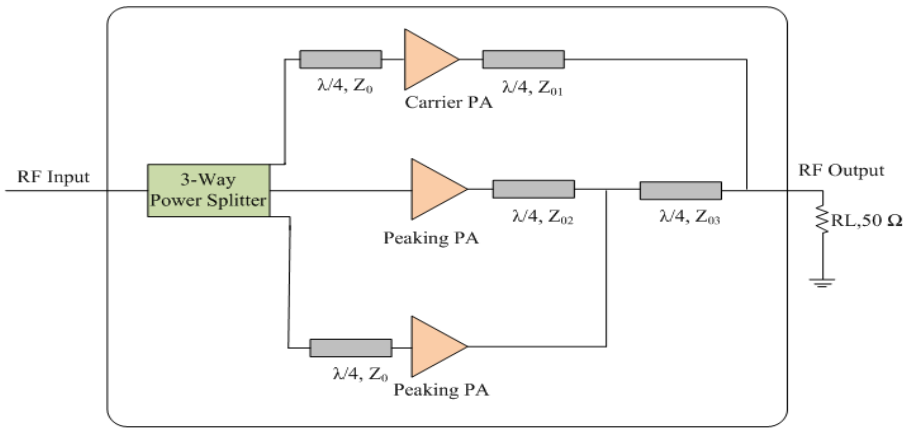


Fig.5. 3-stage DPA with a Modified Combining Approach

3. Modified Output Combining Technique with 3-stage DPA

In this paper, output modified combing techniques with 3-stage Doherty design has been used to achieve the optimal performance of both efficiency and linearity keeping the requirement of 39 dBm average output power for the TD-LTE 20 MHz signal. As discussed in the previous section, following are the key advantages of modified output combining techniques along with 3-stage DPA design: (i) It provides better linearity performance without degrading much average efficiency. (ii) The load impedance of Carrier amplifier is changed from $3 \cdot Z_0$ to Z_0, which is similar to 3-stage DPA with conventional approach. Thus, it will provide the uniform gain versus input power level [27]. (iii) Either same or different power rating of peak amplifiers can be used to decide the flexibility of peak efficiency points at various Back-off levels. In this section, mathematical expression of characteristic impedance for output section has been explained including carrier amplifier and both peak amplifiers.

Fig. 6 shows the equivalent circuit of 3-stage modified DPA considering the carrier and peak amplifiers as an ideal current source. Load modulation is conducted by the fundamental current ratio between the carrier and peaking amplifiers. Output impedance of the carrier amplifier is varied according to the load current delivered by the peaking amplifiers. If input voltage is smaller than 1/3rd of peak voltage, the load impedance of carrier amplifier is $3 \cdot Z_0$ due to infinite load impedance of peaking amplifier. Once the peaking amplifier is turned on, the load impedance of each amplifier can be derived by the active load-pull principle as per the equations (1) and (2) [27].

$$Z_c = 3 \cdot Z_0 \quad 0 < \frac{V_{in}}{V_{in,\max}} < \frac{1}{3} = \frac{3 \cdot Z_0}{1 + \frac{I_{peak}}{I_{carrier}}} \quad \frac{1}{3} < \frac{V_{in}}{V_{in,\max}} < 1 \tag{1}$$

$$Z_p = \infty \quad 0 < \frac{V_{in}}{V_{in,\max}} < \frac{1}{3} = (1 + \frac{I_{peak}}{I_{carrier}}) \cdot \frac{Z_0}{3} \quad \frac{1}{3} < \frac{V_{in}}{V_{in,\max}} < 1 \tag{2}$$

where V_{in} is the input voltage and $V_{in,max}$ is the maximum input voltage.

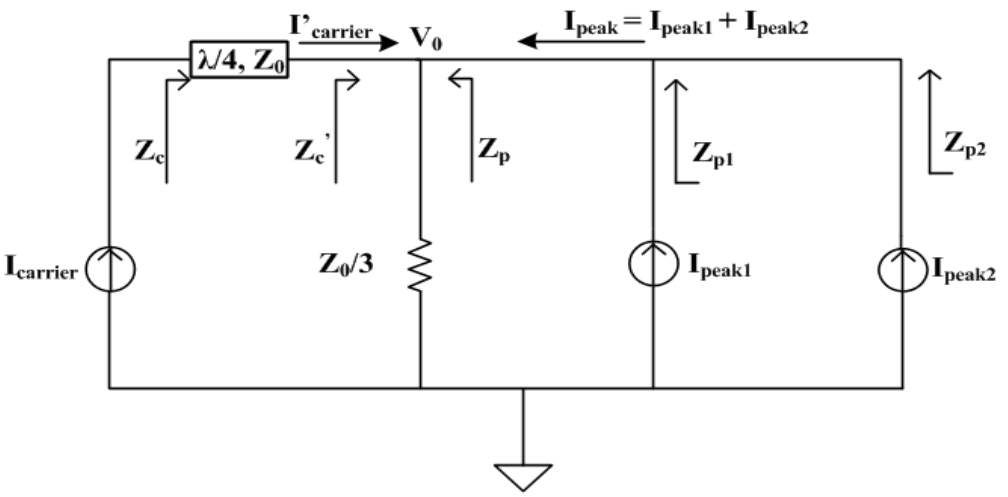


Fig.6. Circuit Analysis in Terms of Ideal Current Source for 3-Way DPA

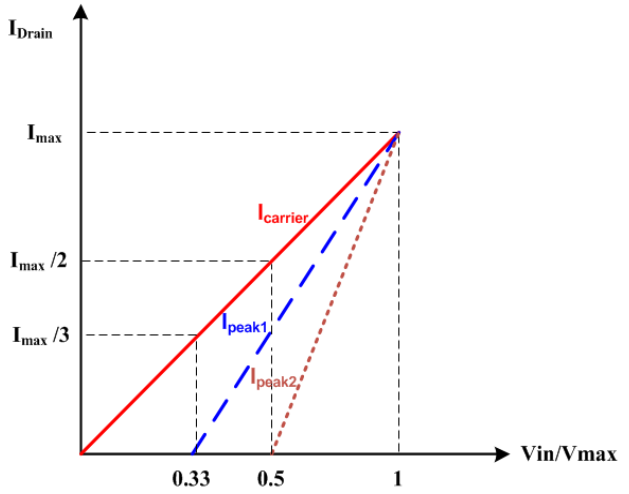


Fig.7. Fundamental Current Profiles of Each Power Amplifier for 3-Stage DPA (1:1:1) With Modified Approach

In the region of V_{in}/V_{max} from 0 to 0.33 V, only the carrier amplifier operates. The carrier amplifier maintains a $3 \cdot Z_0$ load impedance when both peaking amplifiers are turned off. Thus, at the -9.54 dB back-off output power, the carrier amplifier's load-line reaches the knee region of $I_{max}/3$ current level and operates at maximum efficiency. In the region of 0.33–0.5 of V_{in}/V_{max}, the carrier and one peaking amplifier operate. The load impedance of carrier amplifier and first peaking amplifier is converted from $3 \cdot Z_0$ to $2 \cdot Z_0$ and from open to $4 \cdot Z_0$, respectively. The second maximum efficiency point is achieved when the output power is backed off 6 dB from the peak power or the drain current reaches to $I_{max}/2$. Carrier amplifier and both peaking amplifiers are turned on in the region of 0.5–1 of V_{in}/V_{max}. In this case, the load impedances of three amplifiers are converted to Z_0 and current reaches to I_{max} which forms the third peak efficiency point. Impedance values of the carrier and both peaking amplifiers decrease as the corresponding input voltage level increases, which collectively maintains overall uniform gain at DPA output. The values of the impedances used in the $\lambda/4$ transmission lines are as per equations (3), (4) and (5), which are different than the conventional 3-stage Doherty design.

$$Z_0 = 50\Omega = Z_{02} \tag{3}$$

$$Z_{01} = \sqrt{3} \cdot Z_0\Omega \tag{4}$$

$$Z_{03} = \sqrt{\frac{3}{4}} \cdot Z_0\Omega \tag{5}$$

4. Circuit Design and Analysis of Simulation Results

The output power requirement for LTE Micro eNodeB is 5 W (37 dBm) at antenna port. Losses between power amplifier and the antenna port are approximately 1.6 to 2.0 dB due to TDD Isolator, Switch and Cavity Filter. Considering these 2 dB losses, the proposed design of power amplifier is made for 39 dBm average output power.

The input power fed into the circuit is split into three equal parts using a Mini-circuits' SCN-3-28 power splitter. The carrier and peaking amplifiers are designed using Freescale's AFT20S015N LDMOS FET with

15Watt CW power rating. In this analysis, gate bias for the carrier amplifier and peak amplifier is kept as 2.85 V and 1.5 V to drive into class AB and class C mode respectively. As shown in Fig.5, the output power combining is done after the output λ/4 transmission line (Z_{03}) which helps to increase the linear performance of 3-stage modified DPA.

Circuit simulations were performed in Agilent's Advanced Design System (ADS) and SystemVue. ADS is mainly used for DPA design simulations and SystemVue is used for validating the above 3-stage modified design along with DPD to meet the linearity specifications. Fig. 8 explains the output 1-dB compression point (OP1dB) for 3 stage conventional DPA. The OP1dB of the 3 stage modified DPA was found to be 46 dBm as shown in Fig. 9, which is more than 1.1 dB compared to conventional 3 stage DPA. This enables to achieve the 39 dBm average output power for 20 MHz LTE signal. It was not feasible by 2-way, 3-way and 3-stage conventional DPA which is explained in the subsequent section.

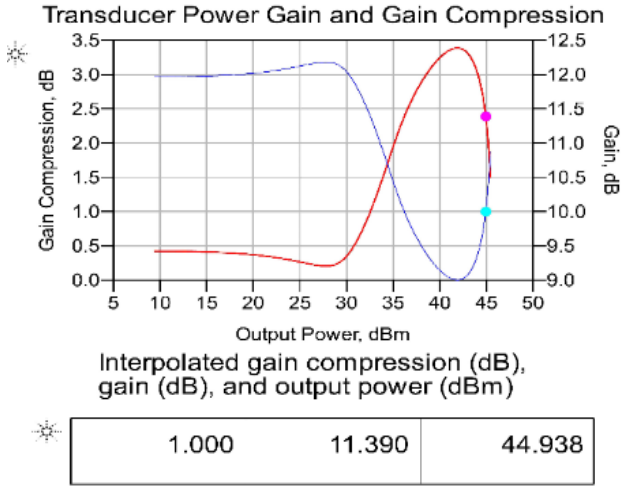


Fig.8. Gain and OP1dB Results for 3 way Conventional DPA

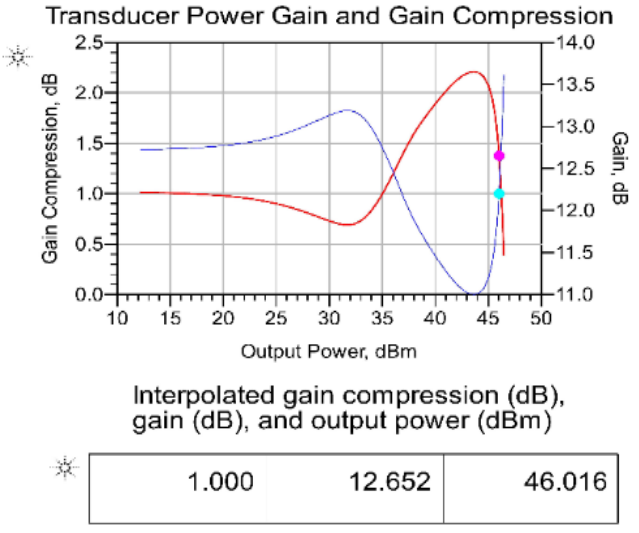


Fig.9. Gain and OP1dB results for 3 way DPA with Modified Output Combining Circuit

As per the simulation results, 3-stage modified DPA has the following advantages: (i) OP1dB increases by 1 dB (ii) Gain increase by 1.3 dB (iii) Gain Flatness increases by 1.5 dB with respect to different power level and (iv) Efficiency increases at 8-9 dB back-off. Fig. 10 and 11 depict the efficiency comparison for single device Class AB PA, 2 way DPA, 3-stage conventional DPA and 3-stage modified DPA against various back-offs from the OP1dB and average output power respectively considering 20 MHz LTE signal. From the below two figures, it can be deduced that modified DPA and conventional DPA have similar efficiency at corresponding back-off but due to better linearity modified DPA is able to provide average output power of 39 dBm.

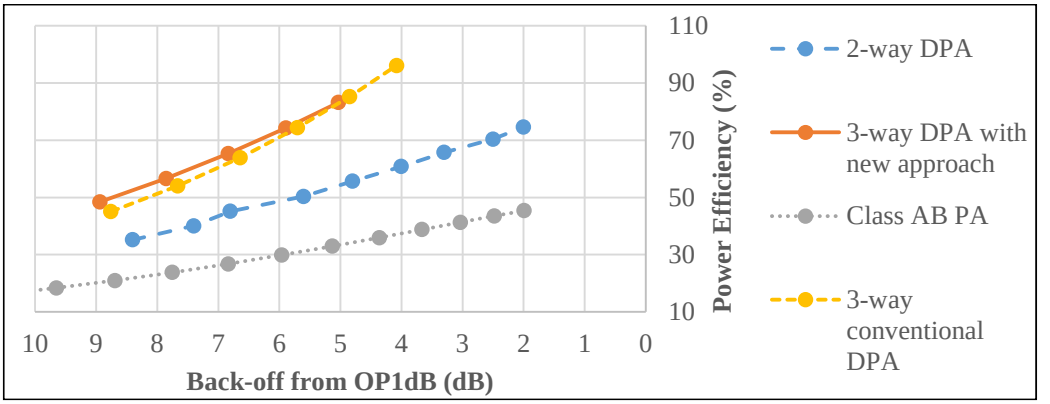


Fig.10. Efficiency Comparison for Different PA Configurations With Respect To Back-Off

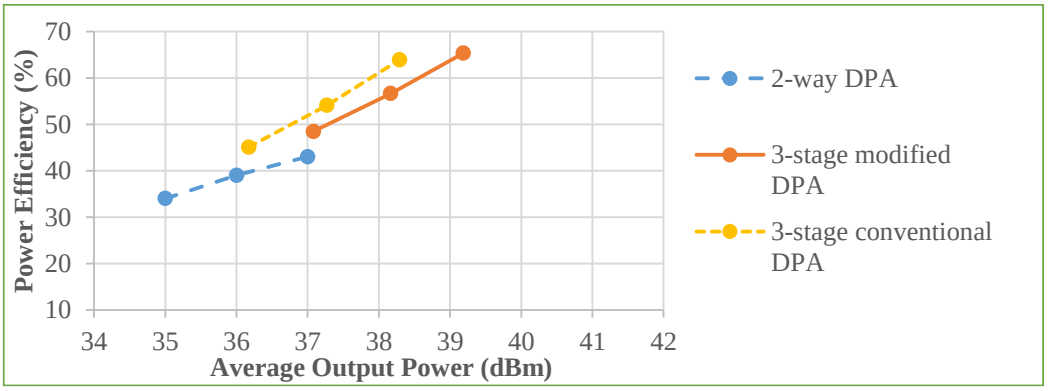


Fig.11. Efficiency Comparison for Different PA Configurations With Respect To Average Output Power

As a next step, the design is simulated with an LTE downlink signal to find the Adjacent Channel Power Ratio (ACPR) in the ADS. ACPR value degrades from class AB single device, 2 way DPA, 3-stage DPA as transistor will operate very close to saturation region. It increases the efficiency but at the same time decreases the linearity performance. Table 1 explains the performance achieved using the 3-stage modified DPA for LTE Micro eNodeB application.

Table 1. Performance of 3-stage Modified DPA

Parameter	Unit	Data
Operating band	MHz	2300-2400
Channel Bandwidth	MHz	20
Output power	dBm	39
Efficiency	%	65.3
ACPR	dBc	-48.2
Gain	dB	12
Input impedance	Ω	50
Output impedance	Ω	50

The objective was to design a Doherty amplifier with 39 dBm average output power for 20 MHz LTE signal using 15 watt LDMOS transistor. The performance comparison among various PA configurations is discussed in Table 2.

Table 2. Performance Comparison for Various PA Configurations based on AFT20S015N LDMOS

Parameter	Single device (Class AB)	2 way DPA	3-stage conventional DPA	3-stage DPA with modified combining techniques
OP1dB (dBm)	41.2	43.5	44.9	46.0
Efficiency @ 7 dB back-off (%)	26.6	43.9	60.0	65.3
ACPR (dBc)	-36.4	-28.8	-22.5	-20.5
Output Power (dBm)	34.4	36.8	37.9	39.2

Above table suggests that the maximum efficiency and output power is achieved by using 3-stage modified DPA. It is important to note that 3- stage modified DPA provides 1.3 dB more output power and degrades the ACPR by only 2 dB. This signifies that 3-stage modified DPA provides more output power with better linearity performance. After achieving the desired efficiency, DPD was implemented in the SystemVue and ACPR has been validated using 20 MHz Band 40 TD-LTE signal.

The DPD implementation was performed using SystemVue and ADS co-simulation. SystemVue generates the DPD stimulus and applies on the 3- stage modified DPA designed in ADS. After removing memory effects before DPD correction, ACPR is found to be improved from -20.5 dBc to -25 dBc. After DPD correction, ACPR of -48.2 dBc was successfully achieved as shown in Fig. 12. This satisfies maximum allowable limit of -45 dBc as per 3GPP specification [5].

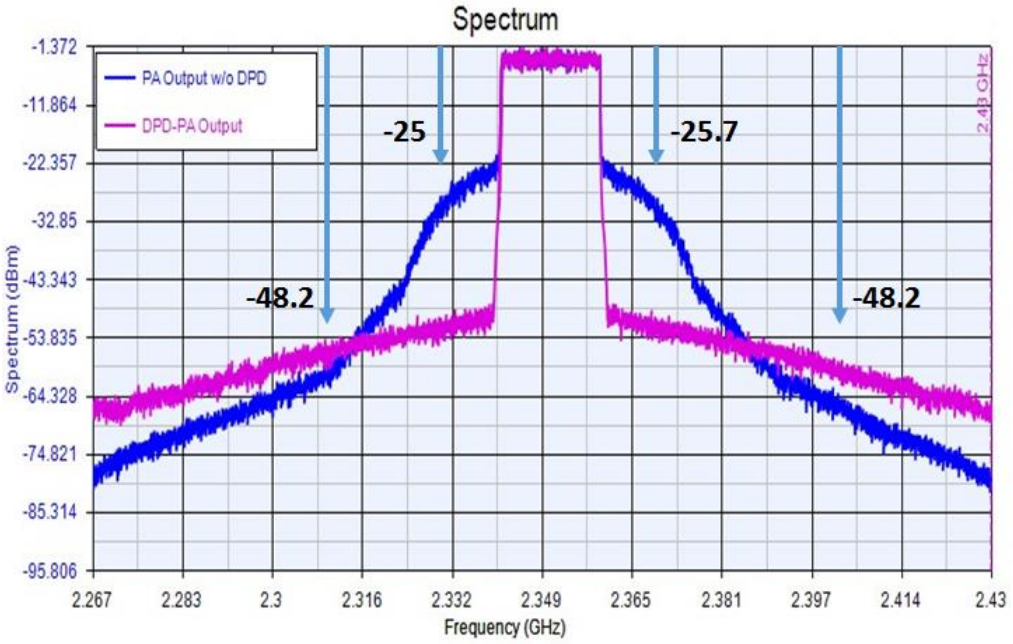


Fig.12. Improved ACPR for 3 way Doherty after DPD

The comparison for the 3-stage modified DPA before and after DPD implementation is summarized as shown in Table 3.

Table 3. Comparison for Proposed 3 Way Doherty Before and After DPD

Parameter	Unit	Before DPD	Before DPD (Removing memory effect)	After DPD
Efficiency	%	65.3	65.3	65.3
ACPR	dBc	-20.5	-25	-48.2
Output power	dBm	39	39	39

The efficiency results achieved for LTE signal is quite promising and encouraging than existing solutions using high power LDMOS transistor for Micro eNodeB.

From Table-2 and 3, it is apparent that low power low cost AFT20S015N device can be used for 5 Watt PA by using DPA with modified combining technique. With other conventional techniques it is impractical to achieve the desired output power level with adequate linearity and high efficiency.

5. Conclusion

In this paper, an efficient 3-stage modified DPA is proposed for 5 watt (37dBm) transmitter power at antenna port of LTE Micro eNodeB. The main advantage of this design is that it uses 15 watt low power LDMOS transistor to achieve the desired target which was not achievable using 3 way conventional DPA. It has also improved the gain by 1.2 dB and gain flatness of 1.5 dB with respect to signal power level. Considering 2 dB

losses between power amplifier and antenna port, the power amplifier has been designed at 39 dBm average output power. An efficiency of 65.3% has been achieved using LDMOS transistor for 20 MHz LTE signal. Linearity requirement for 3-stage modified DPA has been met by achieving ACPR of -48.2 dBc by the successful implementation of DPD using SystemVue. The 3-stage modified DPA configuration has made an economical solution possible with low power LDMOS device AFT20S015N with an advantage of high efficiency.

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