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RF CMOS Low Noise Amplifier Design-A Case Study

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Abstract

A design methodology of Differential Design of CMOS low noise amplifier (LNA) with source degeneration for Bluetooth frequency is presented. The results show that the proposed topology is effective and can be used to achieve the minimum noise figure at all frequencies of interest. This LNA was realized in 0.18μm CMOS technology using Microwave Office Tool from AWR Inc. The measured noise figure is 2.066 dB and the gain is 20.29 dB.

Index Terms: LNA, Bluetooth, Source Degeneration.

1. Introduction

An irreplaceable component of any RF receiver is the front-end low-noise amplifier (LNA). As the first active building block in the receiver front-end, the LNA should provide considerable gain while minimizing the noise introduced to the system. Fig. 1 [6] depicts the simplified structure of an RF receiver front end. As can be seen, the first step of signal amplification is done by the LNA. Therefore, the performance of LNA can greatly affect sensitivity and noise performance [11]of the overall receiver.

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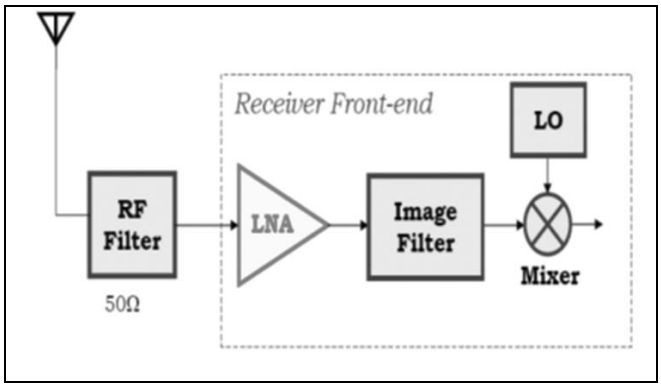

Fig. 1. Receiver Front End

Since the overall noise factor of the receiver front end is dominated by the first stage and can be approximated according to the Frii's formula, [1]

$$NF_{recfront} = \left(\frac{1}{G_{\ln a}}\right)(NF_{subseuent} - 1) + NF_{\ln a} \tag{1}$$

Where $NF_{subsequent}$ is the total input noise factor of the components following the LNA. G_{lna} and NF_{lna} are the gain and noise factor,of the LNA itself. The noise of all subsequent stages is reduced by the gain of LNA and also the noise of LNA is injected directly into the received signal. Thus LNA needs both, high gain and low noise. [7].

1.1. Topology

The general topology of any LNA can be divided into three stages: an input matching network, the amplifier itself and an output matching network. [1].

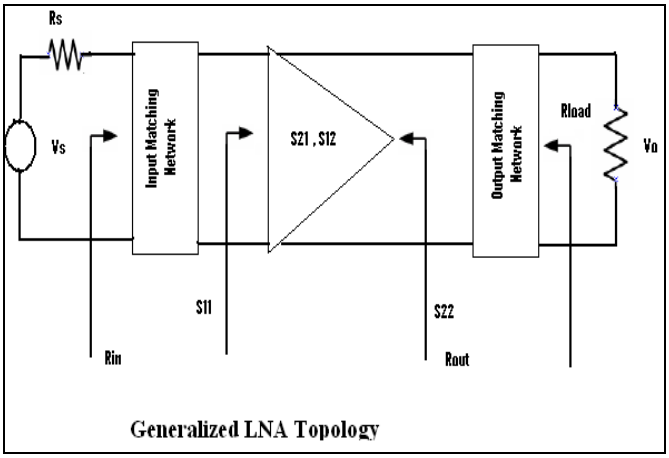

Fig.2. LNA topology

Depicted in the figure 2 are matching networks and s-parameters, which play a significant role in analyzing the performance on Low Noise Amplifier.

The four S parameters are –

S_{21} =Forward gain, Af.

S_{12}=Reverse transmission (or leakage) factor, Ar. This is usually very small in low frequency, but can become significant at high frequency.

S_{11}=Input impedance, Rin, S_{22} = Output impedance, Rout.

The whole design process is carried using the lumped parameters [1], and then the s-parameters are calculated.

To achieve the goal of this paper, out of several topologies, the differential topology [4][6] has been adopted so as to remove the sensitivity to the inductances and to minimize the common mode signal which is described in next section. This section is followed by the calculations of various inductor values and transistor widths for the given gate length and frequency. All these calculations are tabulated in section 4 with a detailed discussion. After this, simulation results have been shown to validate the design. Results for noise figure, gain and s-parameters have been included. Dependency of gain and noise figure on inductors has also been shown. At the end, result summary, showing the comparison with references has been included.

2. Differential LNA

This section describes the theory and design of a CMOS Differential Low noise amplifier. The Design procedure describes the design of LNA using source degeneration technique to provide a good noise match, improved gain & reverse isolation. There are several advantages in using a differential design. Firstly, the virtual ground formed at the 'tail' removes the sensitivity to parasitic ground inductances, which makes the real part of the input impedance purely controlled by the source degeneration inductance (Ls).Secondly the differential amplification of the signal ensures attenuation of the common mode signal. The aim of this paper is to design LNA to work over the Bluetooth frequency band. A summary of the required specification for the LNA is given in Table below.

Table 1. Specifications [2]

Parameter	Specification	Unit
Frequency	2.45 to 2.85	GHz
Noise Figure	< 3.5	dB
Voltage gain	> 20	dB
Power gain	> 10	dB
Source /Load impedance	50	Ohm
Load Cap.	0.4	pF

The design of LNA is carried using Microwave Office from AWR.

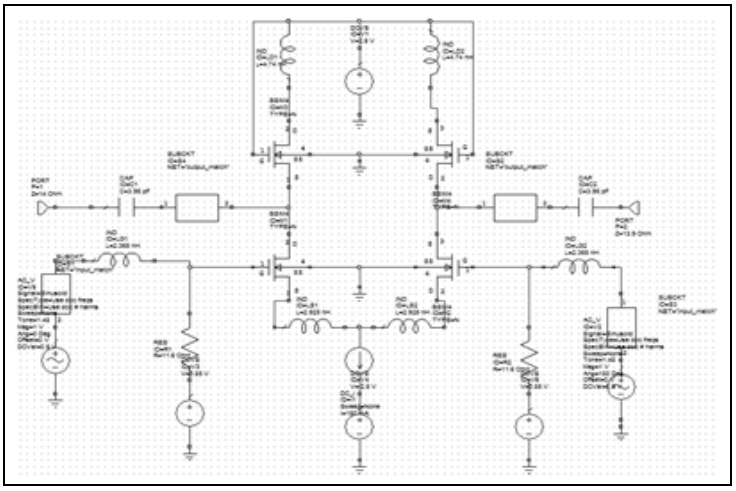

Fig. 3. Differential LNA Design

The inductive degeneration topology is used for impedance matching. [2][5] [15]

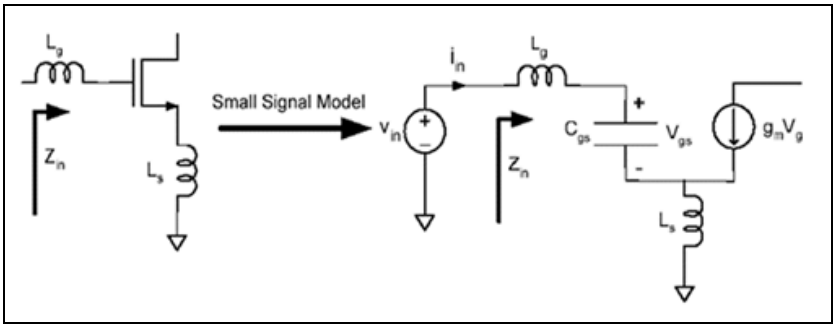

Fig. 4. Small Signal Analysis (Inductive Degeneration)

Referring figure 4 for various parameter calculations[2] the design equations are summarized below:

$$R_{in} = R_g + \left(\frac{L_s g_m}{C_{gs}}\right) + j\left(wLs - \frac{1}{wCgs}\right) \quad \text{Rs=50}\Omega. \tag{2}$$

3. Calculations

3.1. Calculation of Lg and Ls

An another inductor Lg is added in series with the gate to resonate with the Cgs Capacitor. We have ,

$$R_{in} = \frac{L_s g_m}{C_{gs}} \tag{3}$$

R_{in} is chosen as 50 ohms.
The value of Ls is picked and the values of g_m and C_{gs} are calculated to give the required R_{in}.

$$L_g = \frac{Q_L R_S}{w_o} - L_S \tag{4}$$

Where ωo = centre frequency = 2.π. 2.65E^9 = 1.665E ^{10} rad/sec and so f_T is given as

$$C_{gs} = \frac{1}{\omega^2{}_o (L_g + L_S)} \tag{5}$$

Therefore Lg= 11.52 nH

3.2. Calculation of Cgs

$$C_{gs} = \frac{1}{\omega^2{}_o (L_g + L_S)} \tag{6}$$

Thus C_{gs} = 0.4pF

3.3. Calculation of Transistor widths

$$W = \frac{3C_{gs}}{2C_{ox}.L_{\min}} \tag{7}$$

where L_{min} = 0.18 um and T_{ox} = 4e-9, Hence W = 350 μm.

3.4. Calculation of Differential Gain

$$g_m = \sqrt{2K_p \frac{w}{L} I_{ds}} \tag{8}$$

$$\sqrt{\frac{2.170.10^{-6}.650.1.1.10^{-3}}{.18}} = 0.36$$

$$A_{LNA} = \frac{g_m.Q_{LOAD}}{Co.2\pi.2.65E9} \tag{9}$$

So, A_{LNA} = 12.56 and A_{LNA} (dB) = 22.72 dB.

4. Design Summary

Table 2. Design Summary

Parameter	Implemented	Unit
Lbias	8.85	nH
Lg	11.5	nH
W (M1 , M2, M3 & M4)	350	µm
Ls	5	nH

After calculations for various parameters, the component values were taken and simulations were carried. Few of the results were not satisfactory, hence near suitable values were taken and simulation was redone. After repeated simulations those values are listed in table -2 which gives the best result as per the specifications. In few cases the tuning tool available with the software[14], has been tried to get the optimized results. After getting the suitable values of components those values were used and final simulation is done. Hence a small change is observed in the calculated and implemented values. In some cases the optimizer is been applied. At the end satisfactory results were obtained which serves the main purpose of this paper.

5. Analysis and Simulation Results

Various analysis' were performed to validate the LNA Design

5.1. s- Parameter Analysis

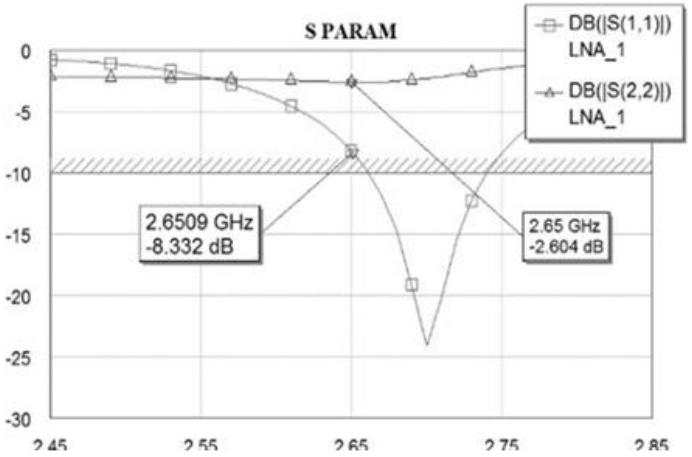

Fig.5. s11 and s22

s- parameters for the design depicts the input and output impedances for the amplifier. The obtained values suites well the design withing the given specifications. The minimum specified values has been shown by the line at the value of -10 dB.

5.2. Gain

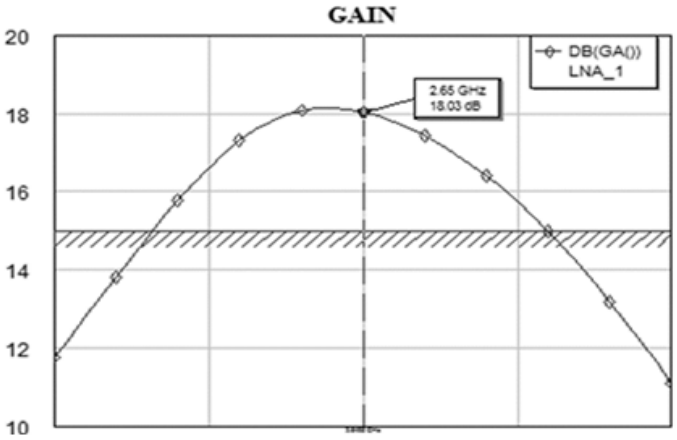

Fig. 6. Frequency Vs Gain

Gain, obtained using the calculated values of parameters was up to the mark, but still there is need of some improvement of design, in terms of improving the overall noise figure of front end, to meet the given specifications.

5.3. Improved Gain

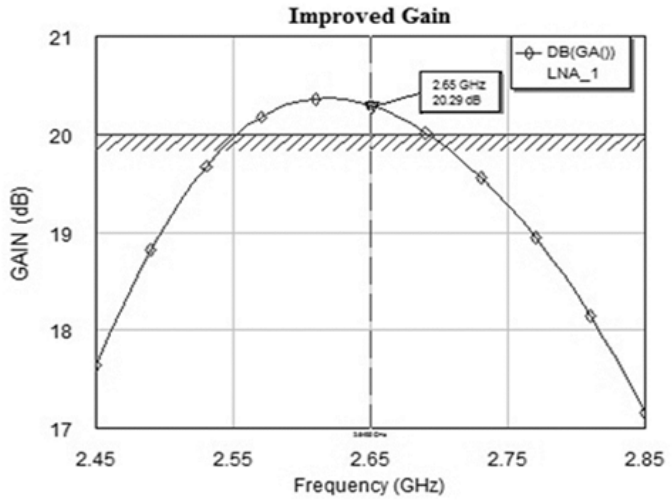

Fig.7. Improved Gain with additional C-S Stage

In order to improve the gain,an additional CS stage [10] [12] have been employed. As a result gain has been improved significantly. The same improvement has been applied in the design to suit the given specifications.

5.4. Noise Figure

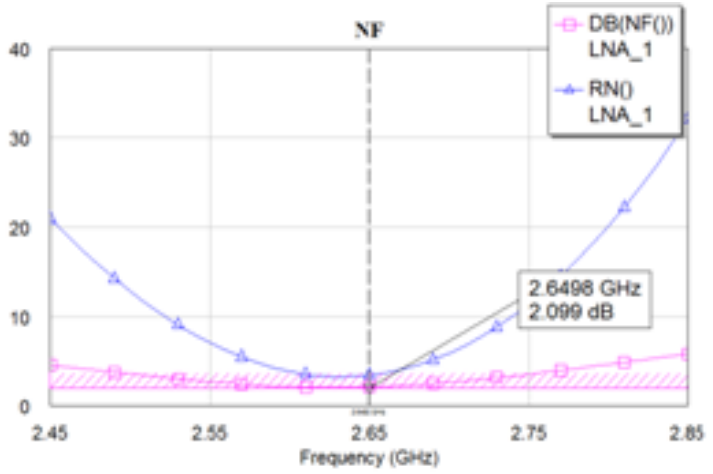

Fig.8. Noise Figure and Noise Resistance(Rn)

As per the Frii's formula, noise figure plays very important role in deciding the overall noise figure of receiver front end. Also LNA should have low noise figure and it should inject less noise to the design.[13]

5.5. Power Gain

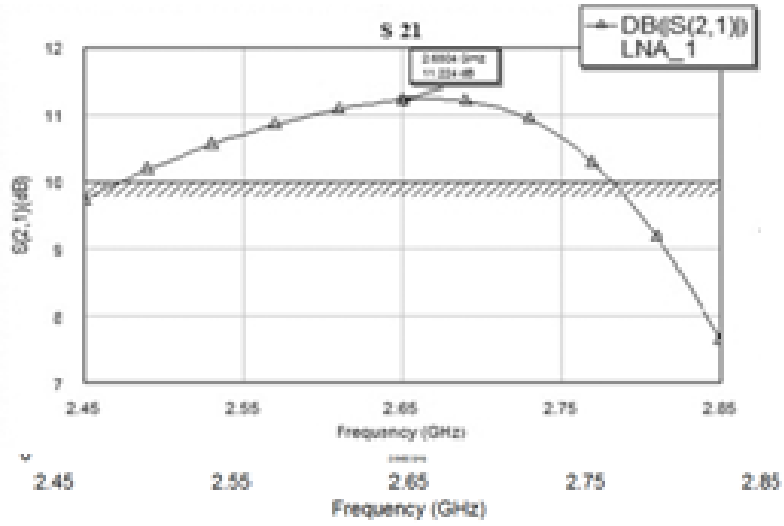

Fig. 9. s-21

Power gain is forward gain A_f. The value of power gain obtained is well above the specifications.

5.6. Bias Inductance Vs. Gain

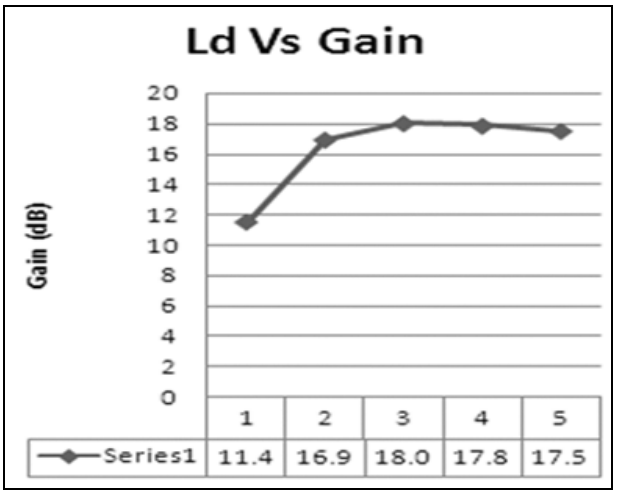

Fig.10. Variation of Gain with Load Inductance(Ld)

Dependence of gain with L_d i.e. load inductance is shown. From the results it can be seen that gain of LNA largely changes with the change in load inductance.

5.7. Lg Vs. Noise Figure

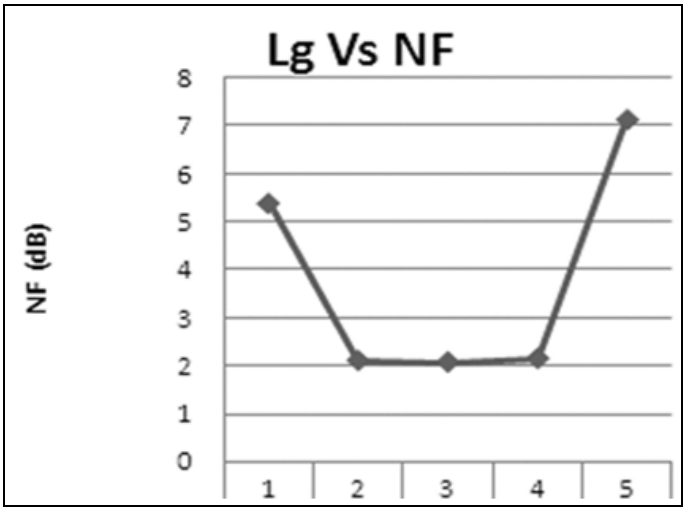

Fig.11. Variation of Noise Figure with Lg

It can be seen that noise figure depends on gate inductance as can be seen. With a small change in Lg noise figure can be changed. Also, gate inductance, in combination with Ls plays very important role in deciding the overall noise figure.

5.8. NFmin, Gmax, Power Gain

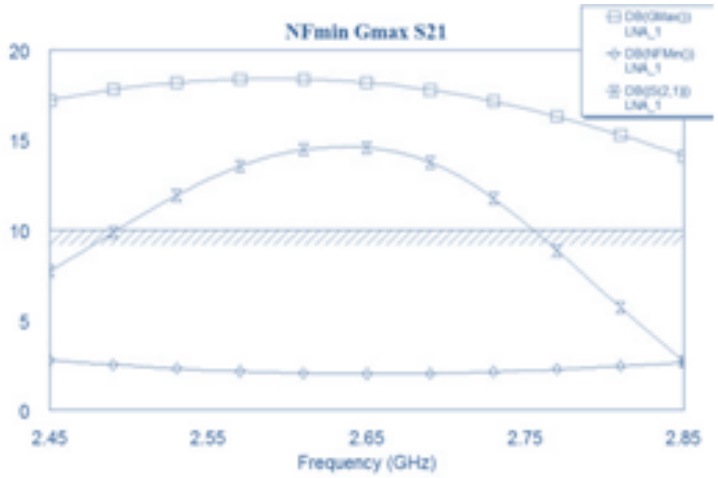

Fig.12: Trade off for NFmin,Gmax and s21

Figure 12 shows the trade off between minimum noise figure, maximum stable gain [9] and power gain of amplifier. Looking at the results it can be seen that variation in power gain and noise figure is linear with respect to frequency, which is well suited for the design.

6. Summary of Results

Table 3. Result Summary

Parameter	**Specifications**	**This Work**	**Unit**
Voltage Gain	>20	20.29	dB
Noise Figure	< 3.5	2.066	dB
Power gain	> 10	11.24	dB
Load Capacitance	0.4	0.4	pF

Table 3 shows the result summary of the design. Load capacitance in combination with load inductance gives the value of gain, which meets the specifications. Noise figure is well within the range so that overall receiver front end noise is reduced.

7. Conclusions

Simulation for circuit is done using AWR's Microwave Office Tool and different plots are obtained for each of the analysis. Most of the specifications are met in terms of Gain and Noise Figure, which are the main focus of this paper.

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Authors Profile

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