

Available online at <http://www.mecspress.net/ijmsc>

## Design Approaches for a Novel Reversible 4-bit Comparator

Harpreet Singh<sup>a</sup>, Chakshu Goel<sup>b</sup>

<sup>a</sup>*M.Tech. Student, Shaheed Bhagat Singh State Technical Campus, Ferozepur, PB, IN (152004)*

<sup>b</sup>*Assistant Professor, Shaheed Bhagat Singh State Technical Campus, Ferozepur, PB, IN (152004)*

---

### Abstract

Reversible logic has shown considerable acceptance and growth in the research fields like quantum computing, Nano computing and optical computing promising lower power dissipation. This paper proposes an optimised design single-bit reversible comparator called SKAR gate with a purpose of reducing quantum cost. Besides, this novel SKAR gate is used as a single-bit reversible comparator to construct an optimised design for a four-bit reversible comparator. The paper discusses two designs, one with the use of SKAR gate and other one using a derivative gate constructed from SKAR gate. Since the reversible logic aims at reducing the value of its fundamental parameters viz. quantum cost, garbage outputs, ancillary inputs, delay and number of gates; Both the proposed designs for single-bit and four-bit reversible comparator are compared with other existing designs on the basis of elementary parameters of reversible logic.

**Index Terms:** Reversible logic, reversible comparator, quantum cost, garbage outputs, ancillary inputs.

© 2015 Published by MECS Publisher. Selection and/or peer review under responsibility of the Research Association of Modern Education and Computer Science

---

### 1. Introduction

According to R. Landauer, a small amount of finite energy is always released in an irreversible operation in which bit(s) being erased [1]. He commented that the energy released or dissipated in an irreversible computation is " $kT \ln 2$ " joules [2]. This figure is not a catastrophe only if it is seen as a single bit erasure. As millions of millions logic circuits are embedded on a single chip of irreversible operational characteristics; this figure becomes quite a challenge for the operational speed and lifetime of the whole circuit.

Furthermore, Gordon E. Moore, co-founder of Intel Corporation, speculated that the number of transistors or circuit elements on a chip will double every two years [3]. As this prediction is self-attesting itself till date, there must be an upper limit on the number of circuit elements that can be embedded on an integrated circuit chip. It is anticipated that a single atom transistor will suffice Moore's law as a size of transistor smaller than atomic scale is, lithographically, unachievable [4]. So, advancements in integrated circuit technology have to be

\* Harpreet Singh. Tel.: +91-9041961411;  
E-mail address: hsr81918@gmail.com

done on a sub-atomic scale and thus a gateway to quantum computing starts to build up.

The above exploration makes a platform to discuss about Reversible Logic and Quantum Computing.

Initially, Reversible logic is supposed to be the new method to the computing world by yielding outputs with lesser power dissipation [5]. The applications of reversible circuits are seemingly quite extensive in quantum computing. Research indicates that reversible logic can prove to be less expensive in terms of power dissipation than conventional irreversible logic with the exponential increase in the number of transistors on a single chip of intact area.

Reversible Logic is a computational logic in which computations done are reversible i.e. time-invertible [5]. The idea is based upon the fact that from elapsing inputs to outputs, no bit must be erased. Every input must reach to at least one output. For Reversible logic to be achieved, some conditions must prevail [6].

- Number of inputs must be equal to the number of outputs. This is mandatory for one-to-one mapping between the inputs and the outputs. Every unique input must have a distinct output. It, therefore, signifies the condition for time-invertibility of the inputs and the outputs i.e. the outputs achieved must be transformed back into the outputs.
- No fan-out is allowed. It generally means that the output should drive only a single forthcoming input. Outputs should not be allowed to load more than a single data line.
- No closed loops or feedbacks are permitted. The outputs should never be connected back to the inputs.

Quantum Computing is that branch of computing in which the computational elementary operations are done by using sub-atomic data carriers [6]. For example, electron spinning in either directions anticlockwise and clockwise, may be justified as basis binary  $|1\rangle$  or  $|0\rangle$ , the ket notation. In quantum computing, the operands on the quantum circuits are called qubits, which in contrast to conventional binary digits used in classical computing, can maintain more than a single state at a given point of time [7]. In case of classical bits, there is only two feasible states '1' and '0'; whereas quantum bits or qubits can maintain themselves in a state of basis binary  $|0\rangle$ ,  $|1\rangle$ , or superposition of  $|0\rangle$  and  $|1\rangle$ . The term basis binary represents the orthonormal basis complex vector of two-dimension space. Superposition of the basis vector  $|0\rangle$  and  $|1\rangle$  is mathematically expressed as  $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$  i.e. the probability of showing a state containing only basis vector  $|0\rangle$  and  $|1\rangle$  is  $|\alpha|^2$  and  $|\beta|^2$ . Quantum computing uses reversible logic as its base to construct quantum circuits which can therefore be elaborated to form application-specific complex quantum circuits.

Comparator is an electronic circuit used to compare two numbers of a given number of bits to return either the numbers are equal or one number is greater than the other one. The existing works have depicted a few reversible circuits which work as comparator and have designed the circuits by using more number of elementary parameters than our proposed work. The quantum reversible logic aims at using the less resources possible and delivering the fast but less power-harnessing computing of the quantum theory. This paper propounds a reversible single-bit comparator named SKAR gate and a four-bit reversible comparator design using instances of SKAR gate and derived SKAR module. The author provides two applications as single-bit and four-bit comparator with an aim for improving the elementary parameters: quantum cost, garbage outputs, ancillary inputs, hardware complexity.

Much work in the field of reversible logic circuits is being done while still its development is in infancy. Examples of this work in the field of nanotechnology are given in [13, 14]. Designs of reversible logic gates like Feynman Gate [15], Toffoli Gate, Fredkin gate [16, 17], Peres Gate [18] can be found in literature.

## 2. Literature Review

As far as the designs of single-bit comparator are concerned:

In [8], the author used five reversible gates out of which two are NG, two FG and a single NLG gate. Also, the ancillary inputs used are 6 in number with a delay of 3 units and 3 garbage outputs. The author used a NLG

gate whose quantum cost is justified to be 2 [6], due to which the total quantum cost of the single bit comparator circuit becomes 26.

In [9], the author put forth a number of comparator designs but only two of those designs are taken in this work. The first design used PG, BJNG and FG gate, one each and delivers output with 5 ancillary inputs, 2 garbage outputs, delay of 3 units, and quantum cost of 10. The second design used one BJNG, one FG and two TG gates producing 2 garbage outputs, 5 ancillary inputs, and delay of 4 units. The circuit is designed with a quantum cost of 16.

In [6], the researcher designed single-bit comparator using a single ZRQC module derived from ZRQG gate. The design is having a quantum cost of 7, single unit delay and single garbage output. The work proposed a ZRQC module which happens to work as single-bit comparator using 2 ancillary inputs while the author has stated it to be 4 [6].

On the other hand, the designs of four-bit comparator specified:

In [8], the proposed four-bit reversible comparator design used 53 gates, 13 units delay, 23 garbage outputs and 59 ancillary inputs. The comparator design's quantum cost is not calculated in the work but it is argued to be 311 as mentioned in [6].

In [10], the design of four-bit reversible comparator was not directly obtained but by using the 8-bit quantum comparator design. The design is justified to be consisting of 32 reversible gates, delay of 15 units, 21 ancillary inputs, 18 garbage outputs, and a quantum cost of 90 [6].

Referring to [6], the author described the use of 4 ZRQC1 modules, 6 Peres gates and 6 Feynman Gates making it a total of 16 reversible gates. Besides, the design produced 20 ancillary inputs, 11 units delay, 17 garbage outputs and total quantum cost of 50 units.

The previous efficient design of a single-bit comparator has two ancillary inputs and single garbage output utilizing 7 units of quantum cost and that of a four-bit reversible comparator, delivers 50 units of quantum cost.

### 3. Proposed Work

The proposed designs of the single-bit comparator and four-bit comparator are justified in this section.

#### 3.1. Reversible Single-bit Comparator Design

A new SKAR gate is shown in fig.1 with its quantum representation in fig.2. The gate is a 4x4 reversible gate which can work as a single-bit comparator by taking two ancillary inputs and giving single garbage output. To show that the new proposed gate is reversible, its truth table is shown in table 1.

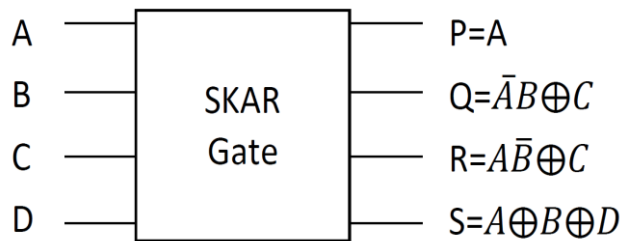


Fig. 1. Reversible 4×4 SKAR gate

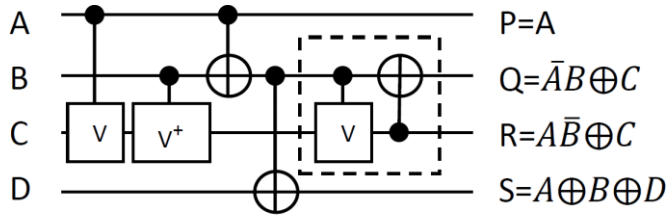


Fig. 2. Quantum Representation of SKAR gate

Table 1. Truth Table of Reversible SKAR gate

Inputs				Outputs			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	1
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

The truth table maps each input of the SKAR gate to a unique output bit pattern. Also, there is no feedback, and number of inputs equal to the number of outputs makes it a reversible gate. Using C and D as ancillary inputs and initializing them to ‘0’ and ‘1’ respectively, the inputs of the comparator are A and B with reference to figure 1. Also, P becomes the single garbage output leaving Q, R and S as the outputs for A<B, A>B and A=B respectively.

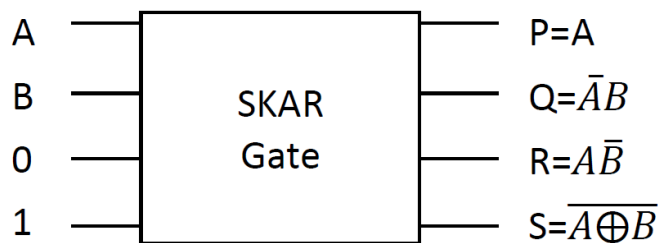


Fig. 3. Working of SKAR gate as single-bit comparator

3.2. Reversible Four-bit Comparator Design

For the design of four-bit comparator, a  $3 \times 3$  gate derived from SKAR gate named SKAR1 gate is used, which itself is also reversible. The gate described here follows the same ideology as used in ZRQC1 module yet difference in basic design representation may be observed [6]. The SKAR1 module, shown in fig. 4, has identical quantum cost with the SKAR gate, the only purpose of using it here instead of its inheritor SKAR gate is to reduce the overall number of ancillary inputs and garbage outputs.

The truth table for SKAR1 module is shown by table 2. For an irreversible four-bit comparator used in conventional digital computing, the truth table is shown in table 3.

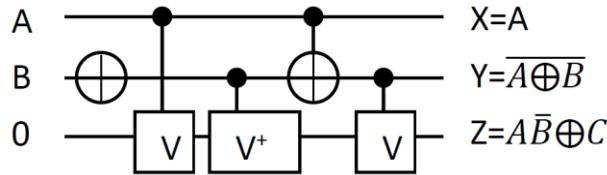


Fig. 4. Quantum Representation of SKAR1 module

Table 2. Truth Table of SKAR1 module

Inputs			Outputs		
A	B	C	Z	Y	X
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	0	0
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	1	1	1

Table 3. Truth table of four-bit comparator

Inputs				Outputs		
A <sub>3</sub> B <sub>3</sub>	A <sub>2</sub> B <sub>2</sub>	A <sub>1</sub> B <sub>1</sub>	A <sub>0</sub> B <sub>0</sub>	A=B	A<B	A>B
A <sub>3</sub> >B <sub>3</sub>	×	×	×	0	0	1
A <sub>3</sub> <B <sub>3</sub>	×	×	×	0	1	0
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> >B <sub>2</sub>	×	×	0	0	1
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> <B <sub>2</sub>	×	×	0	1	0
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> >B <sub>1</sub>	×	0	0	1
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> <B <sub>1</sub>	×	0	1	0
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> >B <sub>0</sub>	0	0	1
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> <B <sub>0</sub>	0	1	0
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	1	0	0

Two designs are proposed here for the designing of four-bit reversible comparator, one using SKAR gate and the other using SKAR1 module inherited from SKAR gate itself.

Design 1. Using SKAR gate as the basic single-bit comparator, four-bit comparator uses 6 Peres gates, 2 Feynman gates and of course, 4 instances of SKAR gate. The arrangement of all these gates in order to provide functioning as four-bit comparator in shown in fig. 5(a).

Design 2. Four bit comparator using SKAR1 module, depicted in fig. 5(b), comprises of the same arrangement as used in design 1; however, the instances of SKAR gate are replaced with equal number of SKAR1 modules in their respective places. As described above both these designs offer same quantum cost but

the latter design uses less ancillary inputs and hence, provides less garbage outputs.

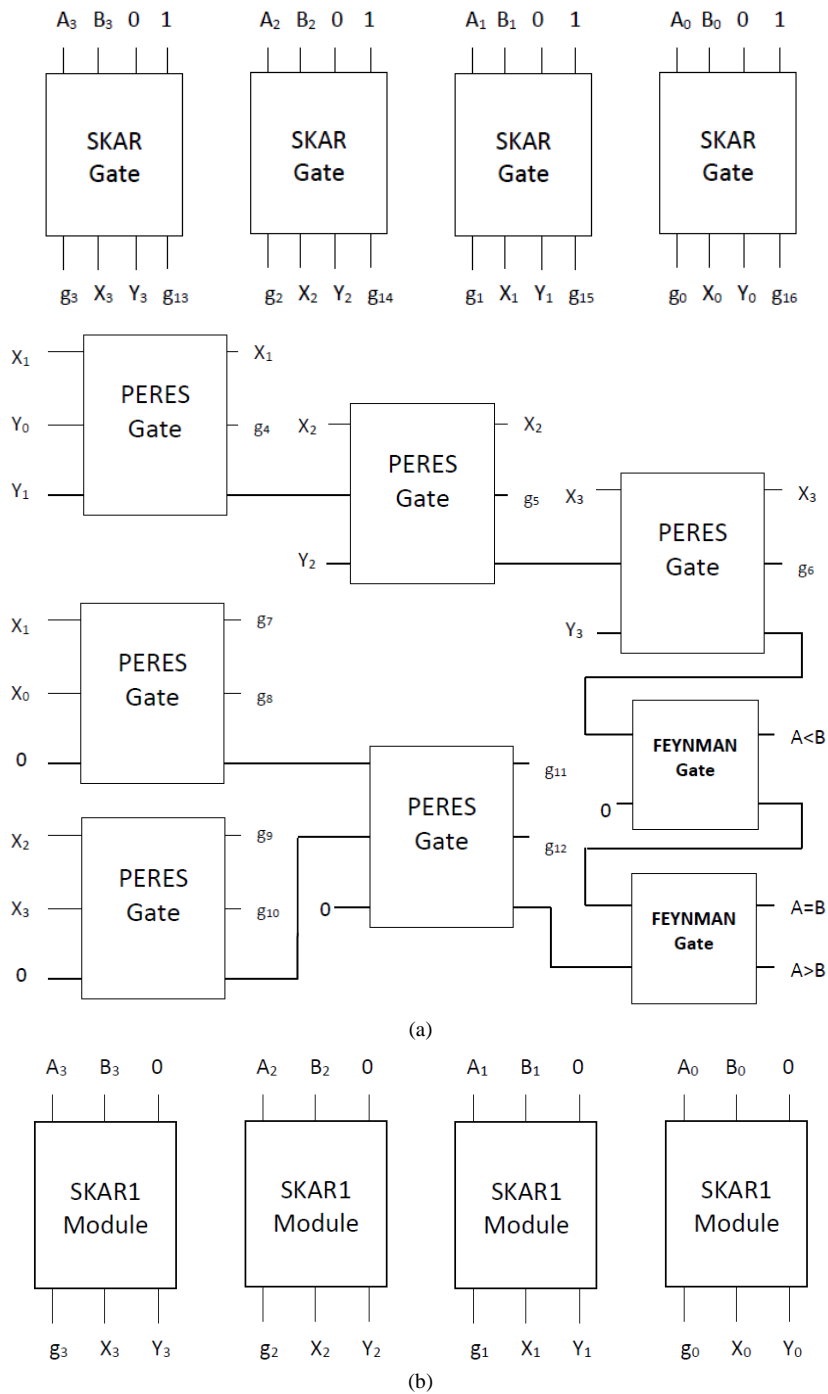


Fig. 5. (a) Design 1: Arrangement of instances of SKAR gate for working as four-bit comparator (b) Design 2: Alternative Arrangement of SKAR1 module in place of SKAR gate in design 1

#### 4. Results and Discussions

The designs for single-bit comparator and four-bit comparator are compared with the previous designs in this section. It has been found that the aforementioned proposed designs are optimized in terms of parameters viz. quantum cost, garbage outputs, ancillary inputs, delay and hardware complexity. The verification and authentication of the designs is stated with valid explanations.

It is postulated that the quantum cost is defined as the number of  $1 \times 1$  and  $2 \times 2$  reversible primitive gates required to design a given reversible circuit. Thus, number of  $2 \times 2$  primitive gates in any given circuit will be the quantum cost of the given circuit [11, 12]. Thus, to justify the stated quantum cost one can just count the number of primitive quantum gates used to make a given circuit and that will be the quantum cost of the given circuit.

It has been observed that the design of single-bit comparator uses two ancillary inputs and produces single garbage output. Also, from the quantum representation given in fig. 2, the quantum cost of SKAR gate is found to be 5. In comparison to the existing designs, the performance parameters of SKAR gate is compared in table 4.

Table 4. Comparison of single-bit comparator with existing designs

Design	Quantum Cost	Delay	No. of gates	Garbage outputs	Ancillary inputs
Existing design[8]	26	3	5	3	6
Existing design1[9]	10	3	3	2	5
Existing design2[9]	16	4	4	2	5
ZRQC module[6]	7	1	1	1	2
<b>Proposed SKAR gate</b>	<b>5</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>2</b>

The quantum cost of SKAR1 module derived from SKAR gate is also found to be 5, which can be verified from its quantum representation given in figure 4.

By contrasting design 1 and design 2 for the four-bit comparator, it is seen that both the designs offer identical quantum cost of 46. But the design 2 uses 8 ancillary inputs; 4 less than that of design 1. Also, the garbage outputs produced by the design 2 are 13 in number, which are 4 four less than those in design 1.

Table 5. Comparison of four-bit comparator with existing designs

Design	Quantum Cost	Delay	No. of gates	Garbage outputs	Ancillary inputs
Existing design[8]	311	13	53	23	59
Existing design[10]	90	15	32	18	21
ZRQC module[6]	50	11	16	17	20
<b>Design1</b>	<b>46</b>	<b>6</b>	<b>12</b>	<b>17</b>	<b>12</b>
<b>Design2</b>	<b>46</b>	<b>6</b>	<b>12</b>	<b>13</b>	<b>8</b>

Thus, both the designs proposed in this paper show improvement in every elementary parameter used in reversible logic synthesis.

## 5. Conclusion and Future Scope

Reversible logic attempts to achieve the functionality provided by the conventional digital computing systems but with the use of less power and resources. Hence, all the necessary components and digital circuitry is being designed using reversible logic. This paper proposes designs for single-bit comparator and four-bit comparator. Both the proposed designs offer improvements in all the aforementioned fundamental parameters used in reversible logic design viz. quantum cost, garbage outputs, ancillary inputs, number of gates and delay elapsed. The improvement in quantum cost is seemingly judged as less power consumption. These design approaches can also be modified to produce designs for 8-bit and 16-bit reversible comparator. Other implementations of reversible logic in fields like nanotechnology are shown in [13,14].

## References

- [1] R. Landauer, "Irreversibility and heat generation in the computational process," IBM journal of research and development, vol. 5, issue 3, pp. 183–191, July 1961.
- [2] R. Keyes, R. Landauer, "Minimal energy dissipation in logic," IBM Journal of Research and Development, vol. 14, issue 2, pp. 153–157, Mar. 1970.
- [3] Gordon E. Moore, "Cramming More Components onto Integrated Circuits," Electronics, pp. 114–117, April 19, 1965.
- [4] F.Q. Xie, L. Nittel, T. Schimmel, et.al. , Phys. Rev. Lett. 93, 128303, Sep. 2004.
- [5] C.H. Bennett, "Logical reversibility of computation," IBM J. Res. Dev., vol. 17, issue 6, pp. 525–532, Nov. 1973.
- [6] Ri-gui Zhou, Man-qun Zhang, Qian Wu, Yan-Cheng Li, "Optimization Approaches for Designing a Novel 4-Bit Reversible Comparator," Int. J. of Theoretical Physics, 52, pp. 559-575, 2013.
- [7] M.A. Nielsen, I.L. Chuang, "Quantum Computation and Quantum Information," Cambridge University Press p. 13, Cambridge, 2000.
- [8] Ni, L., Guan, Z., Dai, X., Li, W.j.: Using new designed NLG gate for the realization of four-bit reversible numerical comparator. In: International Conference on Educational and Network Technology, pp. 254–258 (2010).
- [9] Nagamani, A., Jayashree, H., Bhagyalakshmi, H.R.: Novel low power comparator design using reversible logic gates, Indian J. Comp. Sci. Engg. 2(4), 566-574 (2011).
- [10] Thapliyal, H., Ranganathan, N., Ferreira, R.: Design of a comparator tree based on reversible logic. In:IEEE International Conference on Nanotechnology Joint Symposium, pp. 1113–1116 (2010).
- [11] A.Barenco, C.H.Bennett, R.Cleve, D.P.Divincenzo, N.Margolus, P.Shor, T.Sleator, J.A.Smolin, H.Weinfurter, Elementary gates for quantum computation, Phys. Rev. A52(5) pp. 3457–3467 (1995).
- [12] M.Mohammadi, M.Eshghi, M.Haghparast, A.Bahrololoom, Design and optimization of reversible BCD adder/subtractor circuit for quantum and nanotechnology based systems, World Appl. Sci. J. 4(6) pp.787–792, (2008).
- [13] D.Srivastava, S.N.Atluri, Computational nanotechnology: a current perspective, Comput. Modeling Eng. Sci.3(5), pp. 531–538, (2002).
- [14] J.Cervera, S.Mafe, Multivalued and reversible logic gates implemented with metallic nanoparticles and organic ligands, Chem. Phys. Chem.11, 1654–1658, (2010).
- [15] R.P.Feynman, Quantum mechanical computers, Opt. News 11, pp.11–20, 1985.
- [16] T.Toffoli, Reversible Computing. Technical Memo MIT/LCS/TM-151, MIT Lab. for Computer Science, 1980.
- [17] E.Fredkin, T.Toffoli, Conservative logic, Int. J. Theor. Phys. 21, pp. 219–253 (1982).
- [18] A.Peres, Reversible logic and quantum computers, Phys. Rev. A32, pp. 3266–3276, (1985).



**Authors' Profiles**

**Harpreet Singh** is an M.Tech. Scholar pursuing his Masters in Electronics and Communication Engineering from SBSSTC, Ferozepur. He received his Bachelor in Technology from CT Institute of Engineering, Mgmt. and Technology, Jalandhar in the year 2013 affiliated to PTU, Jalandhar. His interest lies in the field of Reversible Computing, Quantum Mechanics, Digital Computing, and VLSI design.



**Chakshu Goel** is designated as Assistant Professor in SBSSTC, Ferozepur. He received his Masters of Technology in Electronics and Communication Engineering from PTU, Jalandhar. He received his Bachelor of Technology in Electronics and Communication Engineering from GNDU, Amritsar. His area of specialization is VLSI Design.

**How to cite this paper:** Harpreet Singh, Chakshu Goel, "Design Approaches for a Novel Reversible 4-bit Comparator", International Journal of Mathematical Sciences and Computing(IJMSC), Vol.1, No.3, pp.20-28, 2015.DOI: 10.5815/ijmsc.2015.03.03