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An Energy-Efficient and Robust Voltage Level Converter for Nanoelectronics

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Abstract—Low-power design has recently become very important especially in nanoelectronic VLSI circuits and systems. Functioning of circuits at ultra-low voltages leads to lower power consumption per operation. An efficient method is to separate the logic blocks based on their performance requirement and applying a specific supply voltage for each block. In order to prevent an enormous static current in these multi-VDD circuits, voltage level converters are essential. This study presents an energy-efficient and robust single-supply level converter (SSLC) based on multi-threshold carbon nanotube FETs (CNTFETs). Unique characteristics of the CNTFET device and transistor stacking are utilized suitably to reduce the power and energy consumption of the proposed LC. The results of the extensive simulations, conducted using 32nm CNTFET technology of Stanford University indicate the superiority of the proposed design in terms energy-efficiency and robustness to process, voltage and temperature variations, as compared to the other conventional and state-of-the-art LC circuits, previously presented in the literature. The results demonstrate almost on average 35%, 55%, 90% and 68% improvements in terms of delay, total power, static power and energy consumption, respectively.

Index Terms—Nanoelectronics, Carbon nanotube field effect transistor (CNTFET), Low-power design, Voltage level converter

I. Introduction

Low-power design has recently become very important in digital integrated circuits for ultra-low power applications. Function of circuits at ultra-low voltages significantly reduces power consumption. In applications such as micro- and nano-sensors, radio frequency identification and medical instruments implanted in the body battery lifetime is more important than performance. Since the lifetime of battery depends on the average power dissipated by the system, the power supply voltage should be lowered in these applications which leads to considerable reduction of power consumption. An efficient technique is to separate the blocks of the circuits based on the required performance and utilize different suitable supply voltages for the blocks. This is an effective approach for lowering the power consumption without degrading the minimum required performance of a VLSI system. [1]. In VLSI designs with multiple supply voltages (multi-V_{DD}) the signals from the high-V_{DD} (V_{DDH}) island can enter the low-V_{DD} (V_{DDL}) island without any problem. However, there can be a relatively high static current in multi-V_{DD} circuits when a signal with logic '1' from the V_{DDL} island enters the V_{DDH} island and consequently the pull-up network of the input stage in the V_{DDH} area will be weakly ON. In this situation, there is a necessity for a voltage level converter as an interface between V_{DDL} and V_{DDH} islands. Therefore, design of energy-efficient voltage level converters is an important challenge in multi-V_{DD} designs [2].

In addition, another effective low-power design technique at the circuit level is device stacking. In this technique the subthreshold leakage current passes through a stack of transistors which are connected serially. Accordingly, the subthreshold leakage current is considerably reduced due to increasing the effective channel length, suppressing the drain induced barrier lowering and higher V_{SB} which increase the threshold voltage of the stacked device in the OFF state [2].

In addition, scaling down the feature size of MOSFET leads to difficulties such as high leakage current, short channel effects, reduced gate control and high power density. To conquer these serious challenges and physical limitations some alternative nanodevices such as carbon nanotube field-effect transistor (CNTFET), nanowire field-effect transistors (NWFET), Graphene nanoribbon field effect transistor (GNRFET), single electron transistor (SET) and quantum cellular automata (QCA) have been introduced and investigated in the literature [3-7].

Considering these nanodevices, CNTFET seem to be a more feasible alternative due to its operational and structural similarity with MOSFET.

In this study, a CNTFET single supply voltage level converter is proposed which benefits from the unique features of the CNTFET nanodevice such as multiple threshold voltages as well as circuit level low-power design techniques such as transistor stacking.

The rest of the paper is organized as follows: Section II briefly describes the characteristics of CNTFET technology. In Section III, the previous LC designs are reviewed. Section IV describes the proposed SSLC design. Section V includes the simulation results and comparisons and finally section VI concludes the paper.

II. A Brief Review Of CNTFET Technology

Carbon nanotube (CNT) is an allotrope of carbon with a cylindrical structure of graphene sheets bent to form a tube which has unique electrical and mechanical properties. CNT is fabricated in two forms of single-walled CNT (SWCNT) and the multi-walled CNT (MWCNT). The arrangement of carbon atoms in a SWCNT is determined with a two dimensional vector called the chiral vector, which is defined according to equation 1 [8].

$$\vec{Ch} = n.\vec{a}_1 + n.\vec{a}_2 \quad (1)$$

In this regard, $\vec{a}_1$ and $\vec{a}_2$ are unit vectors and the n_1 and n_2 are positive integers which defines some important characteristics of a CNT. Chiral vector has a decisive role in making a CNT metallic or semiconductor. If $|n_1 - n_2|$ =3k ($k \in z$) the CNT becomes metallic and otherwise it becomes semiconductor which can be used as the channels region of a transistor. As the size of the chiral vector of a CNT is equal to its base perimeter, the diameter of the CNT is calculated according to equation 2 [8].

$$D_{CNT} = \frac{\sqrt{3}a_0\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \approx 0.0783\sqrt{n_1^2 + n_1 n_2 + n_2^2} \quad (2)$$

Where, a_0 = 0.142 nm is the bond length of carbon atoms in a CNT. The current-voltage characteristics of CNTFET are very similar to MOSFET and it has also a threshold voltage which can be calculated by equation 3 [8].

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}a_0 V_\pi}{3e D_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)} \quad (3)$$

Where, e is the charge of an electron and Vπ (≈3.033 eV) is the carbon π–π bond energy in the tight bonding model. Three types of CNTFET including CNTFET the band to band tunneling CNTFET (T-CNTFET), Schottky barrier CNTFET (SB-CNTFET) and the MOSFET-like CNTFET [9]. SB-CNTFET shows ambipolar characteristics and has metal source and drain regions and hence there is a large Schottky barrier between the intrinsic CNT channel and metal S/D regions which restrict the usefulness of this device for high-performance and low-power applications. In addition, T-CNTFET operates based on band-to-band tunneling and has a limited ON current. However, MOSFET-like CNTFET demonstrates unipolar behavior. In this device, the source and drain regions are heavily doped CNTs and the CNTFET operates on the principle of barrier height modulation by applying of the gate potential. The conductivity of the channel of MOSFET-like CNTFET is modulated by the gate-source bias [9]. It is also notable that the electron and hole have the same mobility in the CNT structure.

According to equations 2 and 3 by setting a specific CNT diameter based on a specific chirality, determined by the chirality numbers (n_1, n_2), the electrical conductivity and the bandgap of CNTs and consequently the threshold voltage of the CNTFET can be defined. It is worth mentioning that many effective and achievable solutions have already been presented in the literature for growing CNTs with specific chirality and setting the desired threshold voltage for multi-tube CNTFETs [10,11]. In addition, in [12], fabrication of imperfection-immune VLSI-compatible sequential and combinational CNTFET logic circuits has been reported.

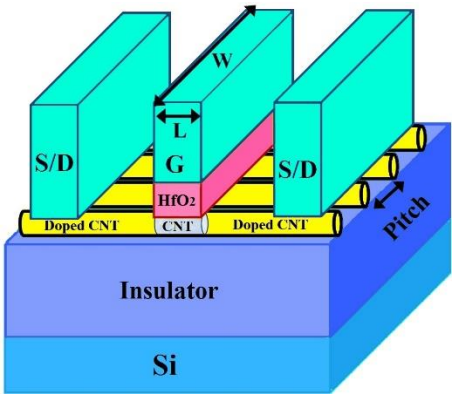


Fig. 1. Schematic of a MOSFET-like CNTFET

III. A Review Of The Previous Works

The dual-supply LC (DSLC) [13], shown in Fig.2(a), is a cross-coupled voltage level converter which requires dual supply voltages, which can increase the complexity of the circuit. In DSLC when the input signal is at logic "0", although the M5 and M3 transistor are ON and charge the node "Q1", the total charged voltage is lower than V_{DDH}. This is because, when the voltage at node "Q1" crosses the switching threshold voltage of the output inverter, the output voltage of inverter (Out) begins to discharge. As a result, before the voltage of node "Q1" reaches V_{DDH}, the output voltage becomes zero. Therefore, the M7 transistor completely turns OFF which makes M11 to be turned OFF and hence, M5 also becomes OFF. In this situation, the node "Q1" is not continuously charged to reach V_{DDH}. However, this incomplete voltage of node "Q1" which is lower than V_{DDH} cannot turn OFF the pMOS transistor of this inverter. Therefore, static power dissipation is increased, and this condition becomes worse by scaling down the technology feature size.

Fig.2(b) demonstrates a single supply LC [14] which uses the stacking technique in its both input and output stages, which reduces the power consumption but increases the delay and area. However, the PDP will not be improved considerably.

The conventional SSLC design [15] shown in Fig.2(c) does not work properly in low voltages especially in the sub-threshold region. In the sub-threshold region, as the gate voltage is lowered, drive current of transistors reduces exponentially. When the input is a low-voltage signal, in the conventional LC, pull-down strength of M1 transistor is weak as compared to the strength of the pull-up transistor (M2). In addition, increasing the gate width of M1 is not adequate for a correct conversion. Moreover, in this design, as the input signal is connected to the gate of p-type and n-type transistors (M1, M2), in low input voltages, both M1 and M2 turn ON, and consequently the static current is increased.

The SSLC design demonstrated in Fig.2(d) [16] utilizes static body-biasing for input n-type transistors to reduce the power consumption. However, this dictates the requirement for separated bodies for these transistors to avoid latch-up problem which destroy the reliability. In addition, the possible presence of overshoot of the voltage (during transitions) can potentially causing the pn-junction diode to be asserted. It is worth mentioning that all the previous LC circuits are redesigned and optimized using CNTFET technology for a fairer comparison.

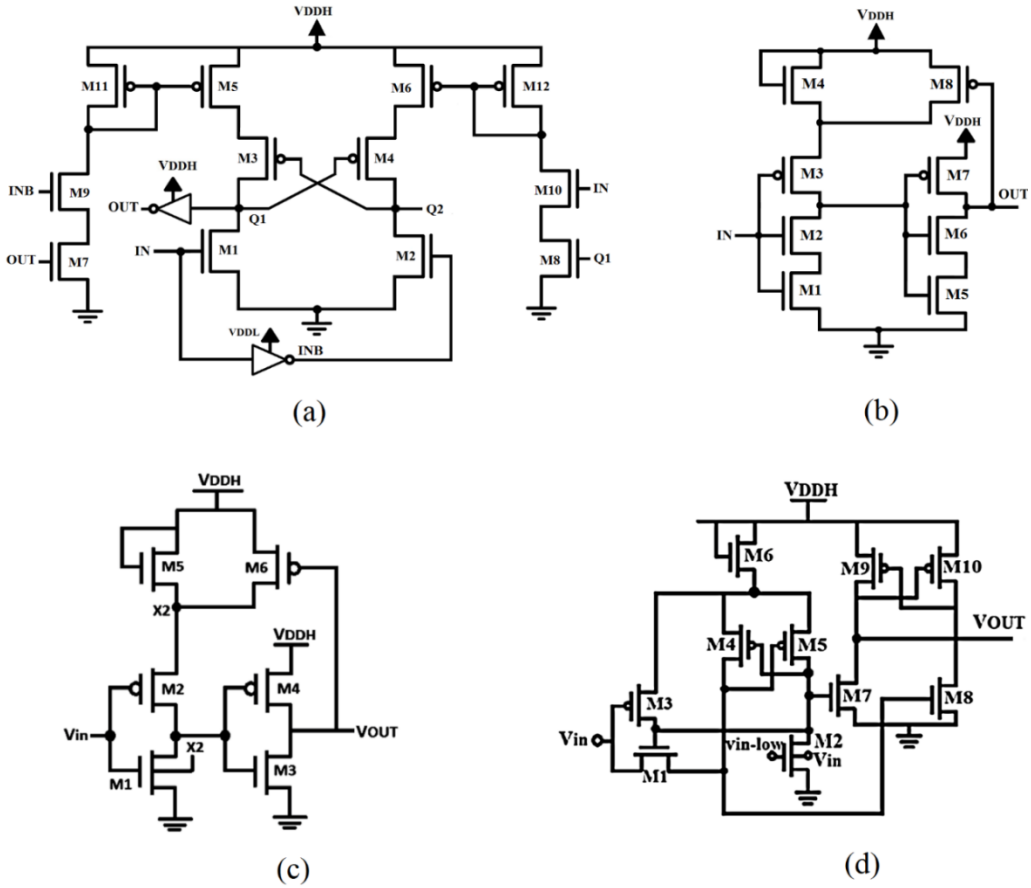


Fig. 2. Previous conventional and state-of-the-art LCs (a) [13] (b) [14] (c) [15] (d) [16]

IV. The Proposed CNTFET-Based SSLC

While, the voltage level converters has a significant role in multi-V_{DD} low-power designs they occupy redundant area on integrated circuits and can impact their overall performance and energy-efficiency. However, while decreasing the power consumption, the minimum required performance of the system should be provided. Therefore, design of a robust LC with very low static power dissipation, lower number of transistors and high performance is an important challenge.

The proposed CNTFET-based SSLC designed based on the Differential Cascode Voltage Switch Logic (DCVSL) is shown in Fig.3. In this design cross-coupled p-type transistors (P1-P4) provide a positive feedback which increase the performance of the circuit. However, in order to reduce the power consumption and to make a trade-off between performance and power consumption stacking technique is utilized in the cross-coupled devices, which leads to a considerable energy efficiency. In addition, using stacking technique and reducing the diameter of the cross-couple transistors considerably enhance the stability and robustness of the proposed DCVSL level converter circuit

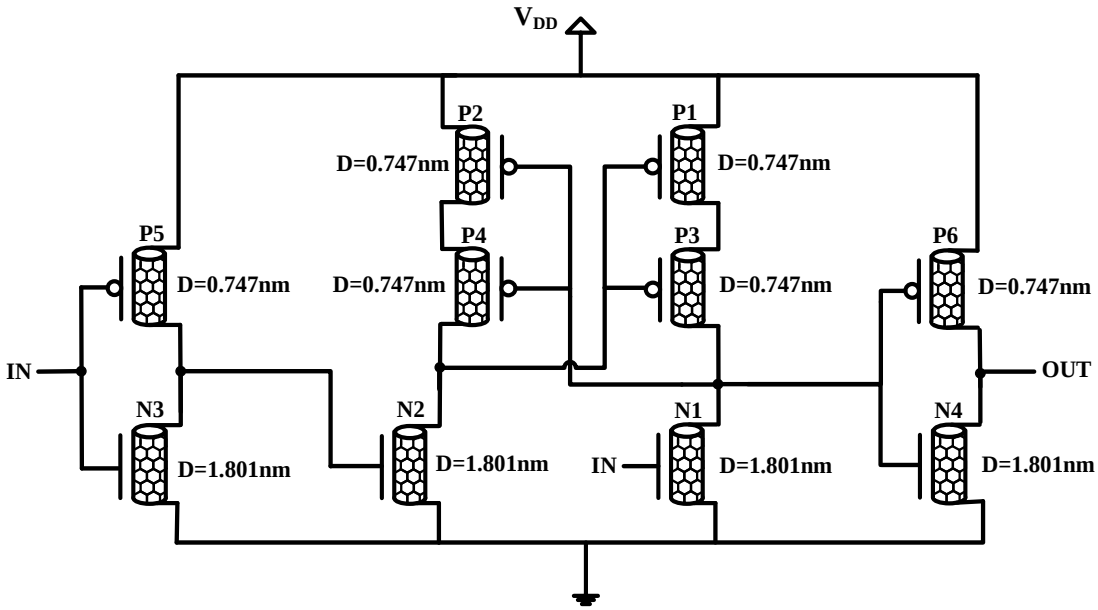


Fig. 3. The proposed level converter

Moreover, as in this design both of low-voltage input signal and its inverse are required, an inverter is utilized (P5 and N3). However, by connecting the low-voltage signal (V_{in}<<V_{DD}) to the input of a common inverter the p-type transistor will be weakly ON, which can considerably increases the power consumption. However, in the proposed single supply design by reducing the diameter of the P3 CNTFET and accordingly increasing its threshold voltage, it will be OFF in this situation and consequently the high static current is totally avoided. At the final stage of the proposed circuit an inverter (P6 and N4) is used to enhance the output driving capability. It is notable that in the proposed design, D_{CNT}/V_{th} are adopted as 0.747nm/0.575V for the p-type CNTFETs and 1.801nm/0.238V for the n-type CNTFETs.

It is worth mentioning that for designing the proposed circuit, only two different CNT diameters, all less than 2 nm, are used. Moreover, all the p-type devices have the same diameter and all the n-type devices have also the same diameter. These features reduce the complexity of the proposed design and considerably enhance its VLSI compatibility and manufacturability.

V. Simulations Results And Comparison

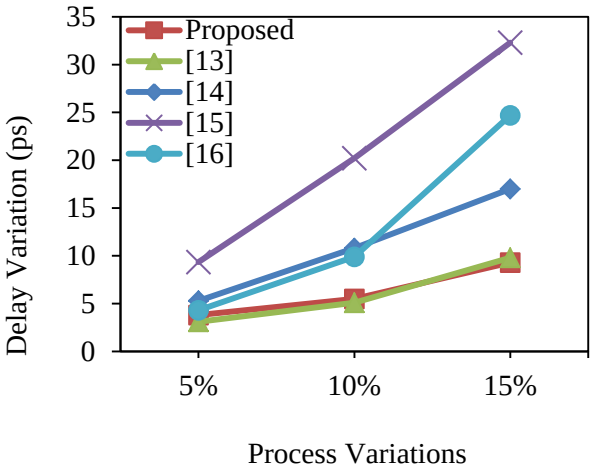
This section examines the proposed SSLC as well as the previous LC designs [13-16] based on the comprehensive MOSFET-like CNTFET SPICE model provided by Stanford University [8] at 32nm technology node. In order to make a fair comparison all of the previous designs are also optimized using the CNTFET technology. The simulation results given in Table 1 demonstrate the overall superiority of the proposed designs as compared to the other conventional and state-of-the-art level converters. It is notable that the cross coupled pull-up devices and the output inverter lead to lower delay and the stacking the pull-up devices reduces the overall power consumption of the proposed design. In addition, the LC of [14] requires double supply voltages while the other designs needs a single supply voltage.

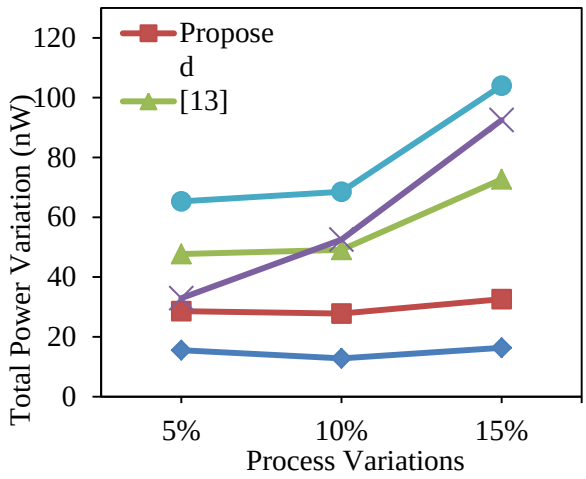
Table 1. The simulation results of the level converters (V_{DDH}=1V and C_{load}=1fF)

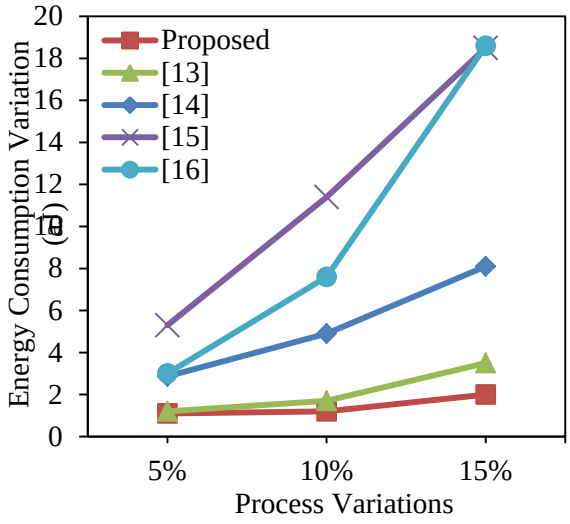
LC	Delay (ps)	Total Power (nW)	Static Power (nW)	PDP (aJ)
V_{DDL} = 0.6V				
Proposed	16.4	181	6.45	2.96
[13]	17.7	230	3.21	4.09
[14]	36.8	478	371	17.6
[15]	33.6	573	382	19.3
[16]	23.9	679	410	16.2
V_{DDL} = 0.7V				
Proposed	16.2	186	5.41	3.01
[13]	15.4	257	3.01	3.96
[14]	36.6	610	496	22.3
[15]	33.1	700	566	23.1
[16]	21.5	794	478	17.1

One of the most significant challenges in nanoscale devices and circuits is sensitivity to random process variations, which can degrade the performance, energy efficiency and stability of the circuits. As the diameter of CNTs under the gate dominantly determine the threshold voltage of a CNTFET device, the function of CNTFET-based designs should be investigated in the presence of CNT diameter variations. Furthermore, variations of the number of CNT under the gate, principally caused by variations in the pitch of CNTs grown on the substrate as well as the variation of the number of surviving CNTs after metallic CNT removal techniques, is proven experimentally to be the dominant source of variation in CNTFET circuits [17]. Accordingly, MonteCarlo transient analysis has been performed to assess these process variations with ±5% to ±15% Gaussian distributions and variation at the ±3σ level.

The maximum variations of the parameters of the LC circuits are shown in Fig.4. The results demonstrate that the proposed cell operate correctly with small parametric variations even in the presence of intensive process variations.







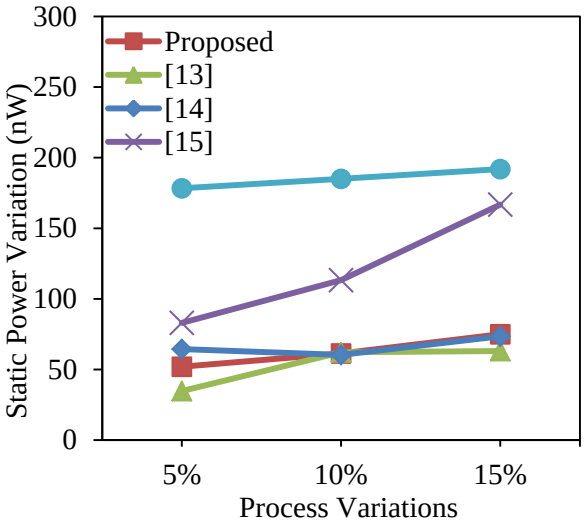


Fig. 4. Parametric variations of the level converters in the presence of major process variations

Temperature variations deviates the performance parameter of the circuits from the expected values and alternate the subthreshold swing and static currents of the devices. Hence, the designs are simulated at a wide range of temperatures from 0°C up to 90°C, to examine their sensitivity to the temperature variations.

The results, illustrated in Fig.5, indicate the low PDP with small variation of the proposed single supply LC in the presence of temperature variations. It is worth mentioning that the relatively small parametric variation of the circuits at different temperatures is mostly due to the CNT thermal stability.

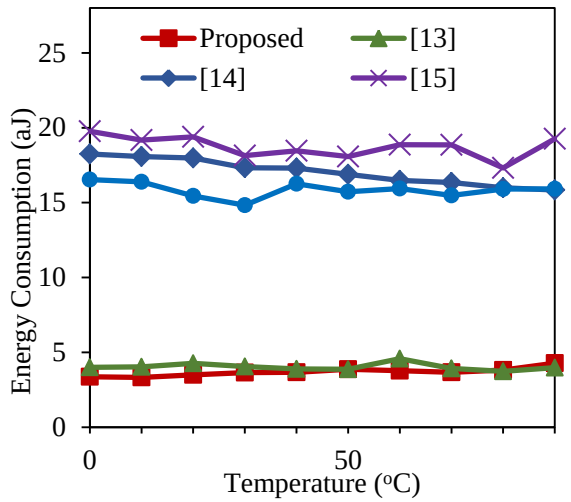


Fig. 5. Energy consumption of the designs vs temperature variations

VI. Conclusions

In this paper a new low-power and high-performance single supply voltage level converter has been proposed for nanoelectronics. The proposed design has benefited from unique characteristics of carbon nanotube FET such as capability of setting the desired threshold voltage by adopting proper CNT diameter. In addition, DCVSL design style as well as device stacking have enhanced the energy efficiency and stability of the proposed design. Extensive simulation results at 32nm technology node have demonstrated the superiority of the proposed design in terms of delay, power, energy consumption and robustness to process, voltage and temperature variations as compared to the conventional and state-of-the-art voltage level converters previously presented in the literature.

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