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A Novel 4×4 Universal Reversible Gate as a Cost Efficient Full Adder/Subtractor in Terms of Reversible and Quantum Metrics

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***Abstract*—**This paper proposes a new 4×4 reversible logic gate which is named as MOG. Reversible gates are logical basic units, having equal number of input and output lines, which can reduce power dissipation in digital systems design through their reversibility feature; because there is a one-to-one corresponding between their input and outputs vectors. The most significant aspect of the MOG gate is that it is a universal gate and has the ability of calculating any logical function on its own. We have also proposed quantum representation of the MOG gate with optimal quantum cost equal to 11. Then, it has been proved that MOG gate can be used to produce a cost efficient reversible full adder/subtractor cell in terms of reversible and quantum metrics. The proposed reversible full adder/subtractor design using MOG gate is a completely optimized circuit in terms of the number of reversible gates, the number of constant inputs, and the number of garbage outputs because it can work with the minimum possible amounts of these reversible metrics. Additionally, it is more efficient than the existing counterparts in terms of quantum cost. The full adder/subtractor cell is an important circuit in VLSI and digital signal processing applications. A lot of works have been done toward designing reversible full adder/subtractors in the literature; but there is no an optimized design with quantum implementation. To prove the applicability of the proposed design in large processing scales, we have constructed 8-bits reversible ripple carry full adder/subtractor circuit using MOG gates. Results have shown the superiority of our proposed design compared with other 8-bits similar designs.

***Index Terms*—**Reversible logic, Quantum Cost, Full Adder/Subtractor cell, Low power design, Reversible metrics.

I. Introduction

Addition/Subtraction is one of the basic structures in many VLSI systems such as microprocessors, digital computing and signal processing systems and nano-micro system [1, 2]. Full adder is one of the most important units in arithmetic circuits, and its performance could affect the efficiency of the whole system [3, 4, 5]. Consequently, it is in the interest of researchers to come up with new ideas so that, their designs have higher performance and low power consumption. One way to ensure having a low power consumption is using reversible computing which has got attention of the researchers in this field.

Reversible logic owes its origin to the basis of thermodynamic concepts in information theory. For the first time, it was ascertained by Maxwell [6] and Szilard [7] that there is a relationship between a single bit of information and corresponding the minimum quantity of entropy. Later in 1961, Landauer [8] pointed out that irreversible processing of information necessarily generates heat and releases it to the environment due to information loss during computation. It was also proved by him that for any bit of information which is erased during computation process, KTLn2 joules of energy dissipates, where k is the Boltzman's constant and T is the absolute temperature at which the computation is carried out.

As information technology have been developing and modern digital systems are needed to afford great deal of computation, designing energy lossless, small and high speed computers is becoming one of the most significant digital architecture requirements these days. According to Moore's law, the number of transistors doubles almost every two years in digital chips [9]. So, the concern for power dissipation as heat generation will be increased if this trend continues to be in effect. In 1973, Bennet demonstrated that reducing heat generation and subsequent energy consumption in the conventional circuits can be avoided by using a new paradigm in digital system designs known as reversible logic [10]. In fact, reversible computing has shown its ability of recovering bit loss by its unique input output mapping, where conventional logic has failed to do so. Reversible logic have intensively drawn prominent attention of researchers in field of ultra-low power green computation, and emerging nanotechnology based systems like

quantum computers [11,12]. Quantum computers are dramatically small and fast devices which benefit from very different information components known as qubits corresponding to the conventional logical bit values 0 and 1. Because any operation performed on qubits is reversible in nature, quantum computer should be constructed by using primary reversible elements such as reversible and quantum gates [13].

In this paper, we have suggested a novel 4×4 universal reversible gate known as MOG which is able to produce the output result of any Boolean function. The quantum equivalent circuit of the MOG gate has also been proposed with the minimum cost of 11 in this work. Furthermore, the proposed gate has been utilized to design one-bit reversible full adder/subtractor cell optimizing reversible and quantum parameters like number of reversible gates, number of constant inputs, number of garbage outputs and the quantum cost as minimum as possible.

In order to prove the efficacy of the proposed design in large scale of digital computing, we have tried to construct an eight bits reversible full adder/subtractor using ripple carry method in which each stage is composed of only one proposed MOG gate as an optimized full adder/subtractor unit. The proposed reversible combinational circuits can be used in designing low power and cost efficient reversible and quantum ALUs, multipliers, dividers and other digital building blocks.

The organization of the paper is as follows: First, the preliminary definitions and basic concepts about reversible logic are discussed in section 2 named as fundamentals part. Section 3 deals with the survey of the existing works in the literature. In section 4, the proposed reversible gate and circuits are presented and discussed in details. Then, results and discussion part, denoted as section 5, includes the comparative results shown in tables as an evidence for superiority of our proposed works in comparison with its existing counterparts in terms of various reversible and quantum metrics. And finally, the conclusion part, which is section 6, summarizes the paper.

II. Fundamentals

The block diagram of an n×n reversible logic gate has been shown in Fig. 1. It has the equal numbers of input and output lines. There is also a one-to-one corresponding between its input vector $I_v = (I_0, I_1, \ldots, I_{n-1})$ and output vector $O_V = (O_0, O_1, \ldots, O_{n-1})$ which causes a reversible gate to be able to recover the input states from the observed output results, and vice versa ($I_v \leftrightarrow O_v$) [14]. Because of this one-to-one mapping among input and output patterns, there is not any bit lost and energy is conserved; hence, no heat is dissipated during computation by means of these gates.

From the point mentioned above, it can be understood that if a circuit is designed using reversible gates, that circuit would be reversible and information lossless. However, synthesis of a logical circuit composed of reversible gates extremely differs from the conventional one because feedback and fan-out paths are forbidden in realization of such circuits [15].

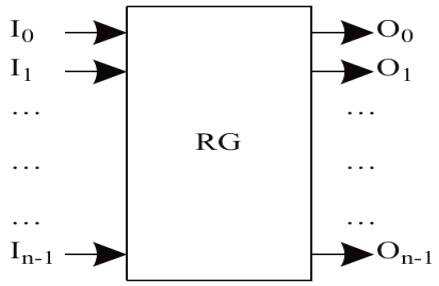

Fig.1. Block diagram of an n×n reversible gate.

In addition, there are some significant cost metrics in the design of a reversible circuit such as the number of reversible gates, the number of constant inputs, the number of garbage outputs and the quantum cost [16]. In order to design a cost efficient and optimized reversible circuit, the primary goal should be focused on minimizing the mentioned parameters as much as possible. The garbage outputs are those output lines which do not perform any useful operation for further computations. In fact, they are just added to the circuit in order to maintain its feature of reversibility. Additionally, constant inputs are lines exist in the input side of a reversible design, which are fixed to a certain logical value 0 or 1, just to serve the desired functionality of the circuit. The quantum cost of a reversible circuit is measured by counting the primitive 1×1 and 2×2 quantum gates like NOT, CNOT, CV, and CV† [17]. In fact, there are three 1×1 quantum gates which can be applied on a qubit as basic operations in quantum computers and represented by (1), (2) and (3) as NOT, V, and V† matrices, respectively.

$$NOT = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \quad (1)$$

$$V = \frac{i+1}{2}\begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix} \quad (2)$$

$$V\dagger = \frac{1-i}{2}\begin{pmatrix} 1 & i \\ i & 1 \end{pmatrix} \quad (3)$$

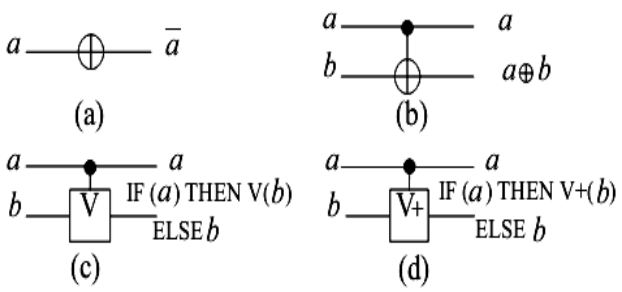

Fig.2. Quantum equivalent circuits of primary reversible gates: (a) 1×1 NOT gate, (b) 2×2 CNOT gate, (c) 2×2 CV gate, and (d) 2×2 CV† gate.

If a qubit of information passes through above gates, then that qubit transforms according to the mentioned

matrices. The quantum cost of these 1×1 reversible gates is assumed to be 0. However, 2×2 reversible gates such as CNOT, CV, and CV† can be built by another inputs as a control line. In such gates, the inputs are passed through the gate on condition that the control input is equal to 0. In contrast, if the control signal is 1, then another input transforms based on mentioned unitary matrices (Fig. 2). These 2×2 reversible gates has the quantum cost of 1.

III. Literature Survey

A number of various reversible gates having different number of input output bits and quantum cost exist in the literature such as 3×3 Fredkin [18], 3×3 TR [19], 4×4 HNG [20], and 3×3 Peres gates [21], etc. the quantum cost of mentioned gate are 5, 4, 6, and 4, respectively. As an example, the quantum representation of Fredkin gate has been depicted in Fig. 3 including 5 elementary quantum gates; and thus its quantum cost equals to 5.

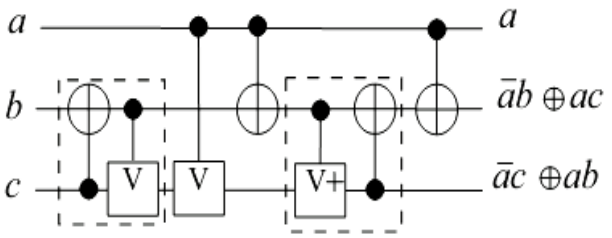

Fig.3. Quantum representation of Fredkin with quantum cost of 5.

Significant contributions have been made in the literature towards constructing reversible logical circuits including combinational and sequential building blocks by using reversible gates. One of the versatile and highly used combinational logic units is full adder/subtractor. A lot of works have been done on designing reversible full adder/subtractor units in recent years. For instance, in [22] authors have proposed three different designs for one-bit reversible full adder/subtarctor using existing reversible gates such as Feynman[23], Fredkin, TR and Peres gates; then they have tried to make three eight-bits ripple carry adder/subtractor using their proposed one-bit circuits. However, their proposed works includes large number of gates, constant inputs and garbage outputs with high quantum cost in some of the cases. Two other structures for reversible full adder/subtarctor cell were introduced in [24] which need high quantity of reversible and quantum metrics. Kaur and Kaur [25] have also suggested another design of full adder/subtractor unit in one-bit and eight-bit scales with ripple carry method which involve high amount of reversible and quantum parameters and are not a cost efficient design. According to our knowledge obtained by the literature review, there is no an optimized reversible full adder/subtractor cell with the lowest possible number of reversible gates, constant inputs, and garbage outputs which provides the quantum implementation with sufficient quantum cost.

IV. Proposed Design

This section consists of two parts. At the first part, we have introduced a novel 4×4 reversible gate and then at the second part, the ability of the proposed gate to work as some logic and arithmetic units will be proved.

A. Novel 4×4 Reversible MOG Gate

Our proposed reversible gate consists of 4 input and 4 output wires and is called MOG. The block diagram of this gate with its outputs functions has been illustrated in Fig. 4. The letters ‘A’, ‘B’, ‘C’, and ‘D’ are used to symbolize the signals which are applied to the gates as input logical values; however ‘P’, ‘Q’, ‘R’, and ‘S’ are considered as output bits and calculated based on determined functions in output lines.

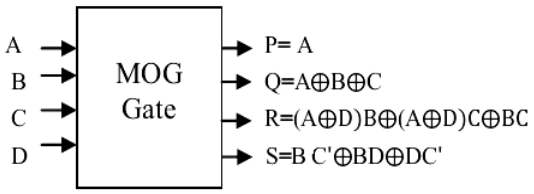

Fig.4. The block diagram of proposed 4×4 reversible MOG gate.

In addition to equal numbers of input and output lines, the reversibility feature of the proposed gate is needed to be proved through its truth table. As the results, we have looked into the all 16 possible patterns of inputs and output vectors belong to MOG gate in Table 1. A one-to-one correspondence between input and output vectors in this table obviously indicates that our proposed MOG gate is reversible since it maps each input pattern to an individual output pattern.

Table 1. Truth Table of the Proposed 4×4 MOG Gate

Inputs				**Outputs**			
A	***B***	***C***	***D***	***P***	***Q***	***R***	***S***
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	0	0
1	1	0	0	1	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1

We have also proposed a quantum equivalent representation for MOG gate in Figure 5. The quantum cost of this circuit is assumed to be 11 because it is composed of 2 CNOT, one Fredkin and one Peres gate [16].

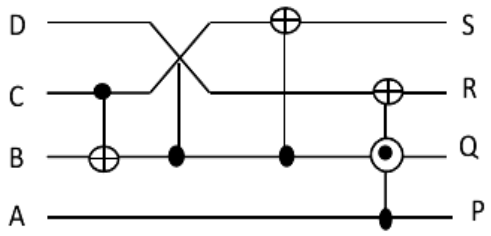

Fig.5. The quantum realization of proposed 4×4 MOG gate

B. Applications of the Proposed MOG Gate

The following subsections present some evidences about the ability of putting our proposed MOG gate into different operation as logic and arithmetic units. We have confirmed that the MOG gate is suited to work as a universal gate, half adder/subtractor, full adder/subtractor, and also can be applied in constructing large scale arithmetic blocks like 8-bits ripple carry full adder/subtractor digital unit.

1) MOG as a universal logic gate

It can be seen from Fig.6 that the proposed 4×4 MOG gate can implement various classical logic operations such as AND, OR, XNOR, NOT and COPY. According to the fact that NOR gate is a universal logic gate and NOR function can be realized by means of our proposed gate (since it can produce both OR and NOT functions), any Boolean function can be implemented using MOG. Consequently, it is hereby declared that the proposed 4×4 MOG gate is a universal reversible logic unit. This is shown in Fig. 6.

2) MOG gate as a half adder/subtractor

In addition to its functionality as a universal gate, the MOG gate can play the rule of half adder/subtractor digital block, as it has been demonstrated in Fig.7. Providing that two bits 'A' and 'B' are used as input data, which the operations is supposed to be carry out on, the "Sel" signal would determine whether add or subtract. In fact, if "Sel" is equal to 0, the MOG gate can work as a half adder; on the other hand, in the case of Sel=1, it will perform subtraction operation. Another input line in this gate is fixed to the '0' logical value and considered as constant input. The output results specify as "Sum" and "Carry Out" bits for half adder and also "Diff" and "Borrow Out" bits for half subtractor in the output lines of the MOG gate. However, the rest of the output lines are not used in any further computation; so they are named g1 and g2 as garbage outputs.

3) MOG gate as a one-bit full adder/subtractor

The full adder/subtrctor unit is a versatile circuit in computer systems architecture and digital signal processing applications. In fact, this combinational logic unit can be used to build other primitive digital building blocks such as multipliers and dividers. Since this digital circuit is placed in the critical path of all processors, designing a cost efficient full adder/subtractor can cause a better performance of complex digital systems. Hence, in this part, we have tried to introduce a novel cost efficient and completely optimized full adder/subtractor in terms of reversible and quantum metrics only by using our proposed 4×4 reversible MOG gate. The proposed one-bit reversible full adder/subtractor is as shown in Fig. 8. Three input bits (A, B, and Cin) are feed to the input lines of the MOG gate and thus the results calculated based on input data are represented by "Sum/Diff" and "Carry/Borrow Out" in form of two individual bits on the output side of the gate. The control input signal, which is labeled as "Sel", differentiates the addition and subtraction functionalities of this structure. It means that if the "Sel" signal is equal to low logical value, the MOG gate performs addition operation. In contrast, for high logical value of "Sel", the structure would act as a subtractor unit. The number of constant input is zero, which is the most ideal and desirable quantity of this parameter for any reversible circuit; furthermore, the number of garbage outputs is 2, represented by g1 and g2, which is impossible to be optimized more than this amount for a reversible design with this functionality. Since the proposed structure used only one MOG gate, the quantum cost of the proposed reversible one-bit full adder/subtractor is 11. We claim that the proposed structure is an absolutely optimized full adder/subtractor cell in terms of reversible metrics since it has the lowest possible number of reversible gates, constant inputs and garbage outputs. Also to the best of our knowledge, there is no an optimized similar structure in terms of mentioned

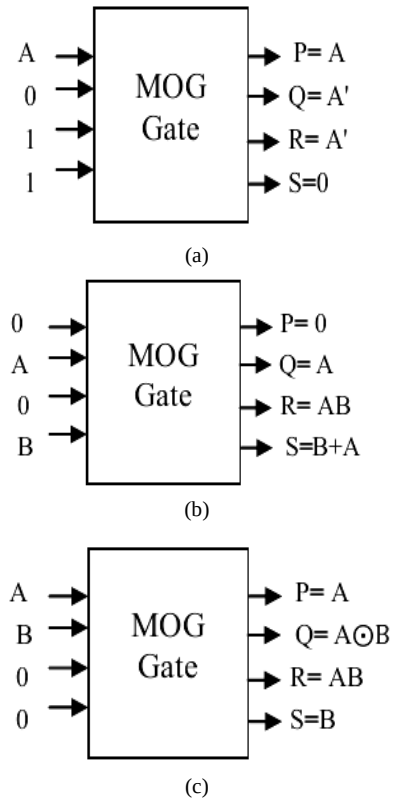

Fig.6. Implementation of various logical functions by using proposed 4×4 MOG gate as a universal reversible gate: (a) NOT and COPY, (b)AND and OR, (c) XNOR and AND.

reversible metrics having the quantum equivalent circuit with the quantum cost lower than 11 in the literature. As the result, the proposed reversible circuit is undoubtedly a cost efficient and optimized full adder/ subtractor cell which can be utilized in constructing low cost reversible and quantum processing units (Fig.8).

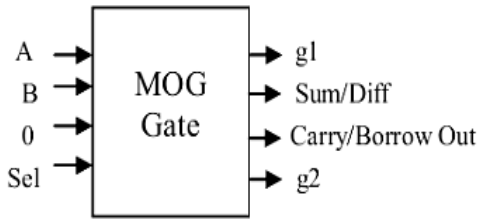

Fig.7. The proposed 4×4 reversible MOG gate as a half adder/subtractor.

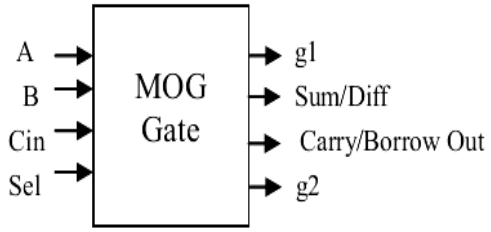

Fig.8. The proposed 4×4 reversible MOG gate as a one-bit full adder/subtractor cell.

4) Designing an 8-bit reversible ripple carry full adder/subtractor

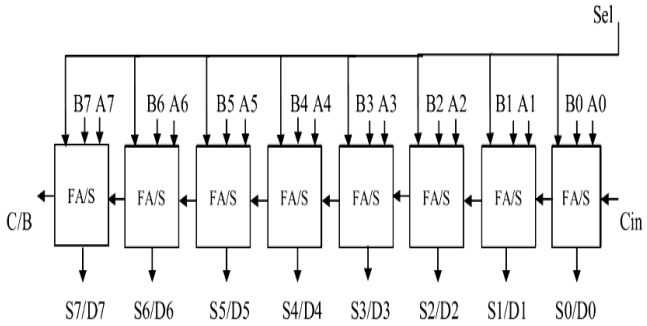

Fig.9. The proposed 8-bits reversible ripple carry full adder/subtractor using MOG gates.

Considering that the proposed one-bit reversible full adder/subtractor could achieve to the optimized number of gates, constant inputs and garbage outputs and also has moderately good quantum cost, we have extended it to the larger scale of computing in form of an 8-bit reversible ripple carry full adder/subtractor according to the Fig. 9. Here, the two 8-bit binary inputs are represented by A0 to A7 and B0 to B7. In addition, the "Sel" signal is used to distinguish 8-bits addition or 8-bits subtraction functions with its logical value equals to 0 or 1, respectively. The carry/borrow signals are obtained after executing the addition/subtraction operations and represented as C/B0 to C/B7 which are conducted from each stage of computing to the next one in the proposed 8-bit ripple carry structure. However, the final 9-bit binary number, which is calculated using the proposed structure, is ascertained by S/D0 to S/D7 and C/B as the output result. The implementation of proposed circuit requires eight full adder/subtractor cells (eight numbers of MOG gate as one bit full adder/subtractor) which results in producing 0 constant inputs, 16 garbage outputs and the quantum cost of 88. This implementation is shown in Fig.9.

V. Results and Discussions

In this section, a comparison between our proposed design and their existing counterparts have been introduced and illustrated. The results are shown in some comparative tables and diagrams. Then, we discussed the results and prove the superiority of the proposed reversible circuits in terms of quantum and reversible metrics against the other similar reversible structures existed in the literature.

Table 2 and Fig.10 shows the results that are obtained by evaluating our proposed one-bit reversible full adder/subtractor unit using MOG gate versus other similar designs introduced in [17, 19, 20]. Obviously, it is evident that our proposed structure includes the lowest numbers of reversible gates, constant inputs and garbage outputs among all the existing counterparts.

Table 2. Comparative results between proposed one-bit reversible full adder/subtractor and the existing counterparts in terms of number of reversible gates, number of constant inputs, number of garbage outputs, and the quantum cost

Designs	Reversible and quantum metrics			
	No. of reversible gates	No. of constant inputs	No. of garbage outputs	Quantum cost
Design 1 [17]	8	3	5	21
Design 2 [17]	4	1	3	14
Design 3 [17]	4	1	3	10
Design 1 [19]	8	5	7	28
Design 2 [19]	10	5	8	24
Design [20]	3	2	4	18
Proposed Design	1	0	2	11

In fact, the proposed structure could bring the number of constant inputs, the number of reversible gates, and the number of garbage outputs to the less desirable amounts equal to 0, 1, and 2, respectively. It has also the minimum quantum cost compared to all the counterparts except the design 3 in [17]. Although the proposed one-bit reversible full adder/subtractor cell in [17] has obtained the quantum cost advantage of just 1 compared to the proposed design in this paper, it is not able to compete with our proposed design in terms of other reversible metrics such as the number of constant inputs, the number of garbage outputs, and the number of reversible gates; because our proposed one-bit reversible full adder/subtractor cell has been designed with the main goal of optimizing all the significant criterion in reversible logic and quantum metrics without imposing any high cost to the other parameters. In fact, the proposed structure has impartially established appropriate proportions for all the comparative parameters as much as

possible.

As a result, it can be considered as a completely optimized structure in terms of all reversible and quantum metrics exist in the table. In addition, a comparison between our proposed 8-bit reversible ripple carry full adder/subtractor and other similar eight-bits structures has been depicted in Table 3 and Fig. 11 in terms of the number of constant inputs, the number of garbage outputs, the number of reversible gates and the quantum cost.

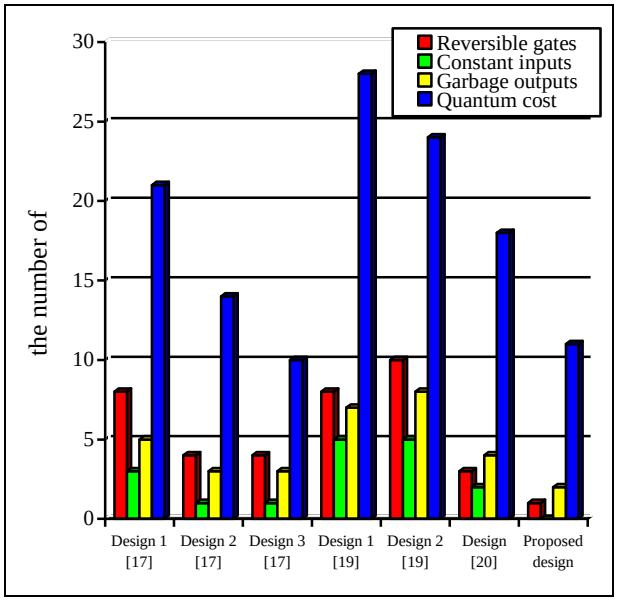

Fig.10. Comparative results between proposed one-bit reversible full adder/subtractor and the existing counterparts in terms of number of reversible gates, number of constant inputs, number of garbage outputs, and the quantum cost.

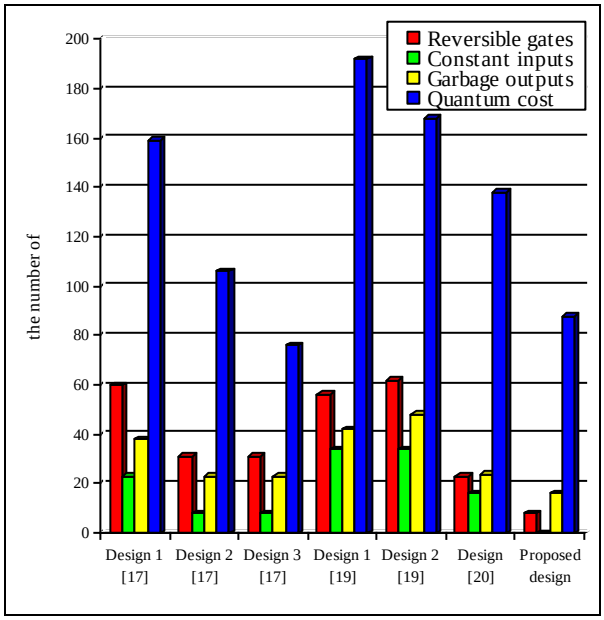

Fig.11. Comparative results between proposed 8-bits reversible ripple carry full adder/subtractor and the existing counterparts in terms of number of reversible gates, number of constant inputs, number of garbage outputs, and the quantum cost.

Table 3. Comparative results between proposed 8-bits reversible full adder/subtractor and the existing counterparts in terms of number of reversible gates, number of constant inputs, number of garbage outputs, and the quantum cost.

Designs	Reversible and quantum metrics			
	No. of reversible gates	No. of constant inputs	No. of garbage outputs	Quantum cost
Design 1 [17]	60	23	38	159
Design 2 [17]	31	8	23	106
Design 3 [17]	31	8	23	76
Design 1 [19]	56	34	42	192
Design 2 [19]	62	34	48	168
Design [20]	23	16	24	138
Proposed Design	8	0	16	88

The results also show the superiority of our proposed 8-bit circuit compared to other existing structures in optimizing all the metrics considering a trade-off between reversible and quantum parameters specially the quantum cost.

VI. Conclusion

Reversible logic has found promising applications in various fields of study such as low power digital designs, quantum computing, digital signal processing and nanotechnology based systems, in recent years. We have proposed a new universal 4×4 reversible logic gate named as MOG which is able to work as various digital reversible building blocks like half adder/subtractor, one-bit full adder/subtractor cell, and 8-bits ripple carry full adder/subtractor circuit.

The quantum representation of MOG gate have been also designed with the minimum possible quantum cost of 11. It has been proved via comparative tables that our proposed reversible full adder/subtractor units, in both one-bit and 8-bit scales, totally improve in terms of the reversible and quantum metrics such as number of reversible gates, number of constant inputs, number of garbage outputs, and the quantum cost compared to the existing counterparts. In addition, the proposed one-bit reversible full adder/subtractor has achieved to an optimized quantity for each of significant criterion even by its own, in this manner.

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