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An Optimized Approach towards Reversible Adder/Subtractor Design on QCA

Snigdha Singh
Electronics and Communication Engineering Department
Institute of Engineering and Technology
Lucknow, India
Email: snigdhas.03@gmail.com

Abhinay Choudhary
Electronics and Communication Engineering Department
Institute of Engineering and Technology
Lucknow, India
Email: svashuc@gmail.com

Manoj Kumar Jain
Electronics and Communication Engineering Department
Institute of Engineering and Technology
Lucknow, India
Email: mkjain71@gmail.com

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***Abstract*—**In the present era of miniaturization, higher power dissipation in form of heat has become a very critical issue for the digital Circuits. This excessive heat may result in the lower chip reliability and even destroy it. Due to this reason a substitute is required for the traditional CMOS technology, Reversible logic is a paradigm in this direction. This paper encompasses of the newly proposed SA reversible logic and basic combinational implementations using a single SA building block only resulting in lower circuit level complexity as well as hardware requirement. The output responses and energy dissipation of proposed SA reversible logic are verified and calculated with the help of QCADesigner and QCADesigner-E simulation tools respectively.

***Index Terms*—**Quantum cost, garbage output, constant input, reversible logic, low power CMOS Technology.

I. Introduction

Reversible Logic [1] is such digital logic which defines corresponding deducibility between input and output vectors. As per Moore's law [2], number of transistors on circuit doubles every 18 months. But according to the physicist Michio Kaku theory, the Moore's law is collapsing in such a way that in the next decade the exponential rise in the computer chip will result in the flattening due to the two major issues namely heat and leakage and Rolf Launder's [3, 4] stated that the heat dissipation occurs due to irreversible nature of components used which can be approximated as kT ln2 that supports the Michio Kaku theory. Further C. H. Bennett [5] enlightened that the heat dissipation can be evaded in fact ruined if the computation is bijective in nature i.e. unique mapping must exist between input–output vectors. If we consider a conventional Ex-OR gate truth table (Table 1) then we can observe clearly that input can't be obtained from output. In case output is 1 then input vector maybe either (0, 1) or (1, 0) which results in the ambiguity of the result. For the sake of resolving this ambiguity a set of additional lines are required which can be estimated as $\ln_2 \mu$. Where, μ is the maximum output overlapping.

In this case μ=2 therefore on substitution in (1),

$$\ln_2 \mu = \ln_2 2 = 1 \quad (1)$$

Table 1. Exclusive-OR Gate Truth Table

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

On taking an additional output line unique input-output pattern can be obtained illustrated in Table 2.

Table 2. Reversible EX-OR Gate (Feynman Gate)

A	B	P=A	Q=A⊕B
0	0	0	1
0	1	0	1
1	0	1	1
1	1	1	0

Various reversible libraries like Tof80, FT 82, Per 85 and Nc00 have been proposed for constructing reversible circuits [6].

The remaining paper is arranged as section II focuses on basic background of QCA along with key terms of reversible design in Section III. The proposed SA logic along with simulation results in section IV and section V respectively, finally section VI gives emphasis on the conclusion.

II. QCA

QCA stands for Quantum Dot Cellular Automata [7] is a renowned technology for digital circuit design and an effective substitute for the semiconductor based technologies because of no power loss during signal transition and propagation. The primitive unit of QCA is QCA cell consisting of four quantum dots arranged in square fashion and two free electrons which tunnel between these dots. Two Charge configurations exist in it as polarization P = 1 and P = -1.

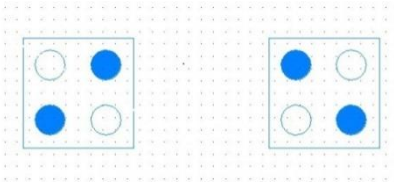


Fig.1. P = 1 and P = -1

Fig.1. explains the electron position in case of P = 1 and P = -1 polarization. Fig.2. enlightens the basic majority gate used for design F (A, B, C) = AB+BC+CA as well as AND gate (set C=0), OR gate (set C=1) using it.

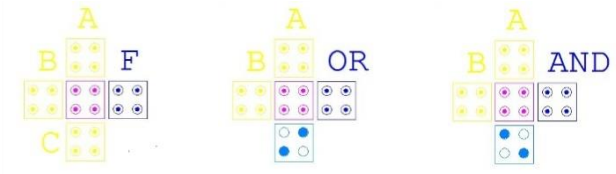


Fig.2. Majority Gate, OR, AND on QCA

QCA requires clocking mechanism for both combinational as well as sequential circuits which completely differ from traditional VLSI technology as prior one require clocking for only sequential circuits. Fig.3. illustrates four states of operation termed as switch, hold, release and relax lagging by π/2 in phase.

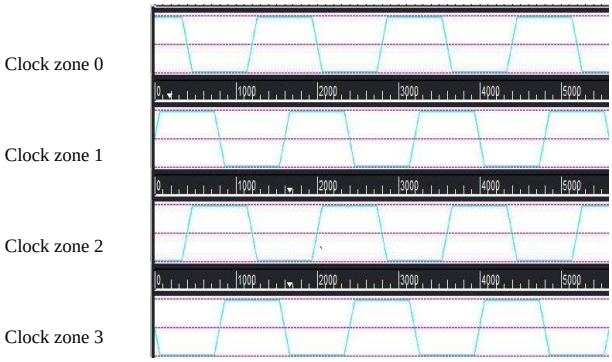


Fig.3. Clock zones in QCA

It's being treated as the most efficient way to design reversible logic gates on ground of area and power efficiency.

QCA wire can be said to be a clump of arranged cells holding same polarization and information flow between input and output due to the coulomb force of attraction acting in between them. Basically two QCA wire configuration exist in QCA [8] such that one is 90 ° and another is constructed by 45 ° cells.

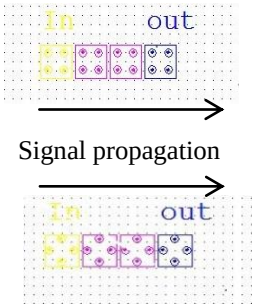


Fig.4. Normal Array or 90 °QCA Wire and inverter Chain or 45 °Wire

III. Key Terms

Constant inputs/Ancilla inputs: Specific set of input vectors set to binary 0 or 1 for circuit implementation is called constant inputs.

Garbage output: Additional output added in such a way that number of elements in input and output vectors become equal is called garbage output.

Quantum Cost: Quantum cost is the number of primitive gates (NOT, CNOT, V and V+) used in the design. Where, V is the square root of NOT and V+ is the hermitian of V following these axioms:

$$V * V = NOT \tag{2}$$

$$V+ * V+ = NOT \tag{3}$$

$$V * V+ = V+ * V = 1 \tag{4}$$

Alternatively, $area*latency^2$ in quantum dot cellular automata also calculate quantum cost [9].

Flexibility: Flexibility can be termed as the how efficient a reversible logic is for performing several logical functions.

Delay: Delay is the maximum number of gate between input and output (on assumption of unit time taken by each gate for computing).

IV. Proposed Circuit

As per the requirement of lower garbage output, reduced area as well as complexity, a new reversible logic as per my survey named SA has been proposed here. It is basically a 4*4 Reversible Logic consisting of input vector(A,B,C,D) and output vector(P,Q,R,S) shown in fig. 5.

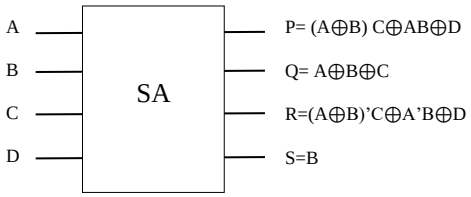


Fig.5. SA Logic Block Diagram

The Truth Table of the proposed logic is expressed in Table 3.

Table 3. Truth Table of SA Logic

A	B	C	D	P=(A⊕B) C⊕AB⊕ D	Q=A⊕ B⊕C	R=(A⊕B)' C⊕A'B⊕ D	S= B
0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	1	1	0	0
0	1	0	0	0	1	1	1
0	1	0	1	1	1	0	1
0	1	1	0	1	0	1	1
0	1	1	1	0	0	0	1
1	0	0	0	0	1	0	0
1	0	0	1	1	1	1	0
1	0	1	0	1	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	1	0	0	1
1	1	0	1	0	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	1	0	1

On considering the input vector as first set and output vector as another set as well as taking the decimal equivalent of the truth table we will obtain the fig.6, depicting the bijective nature of the logic.

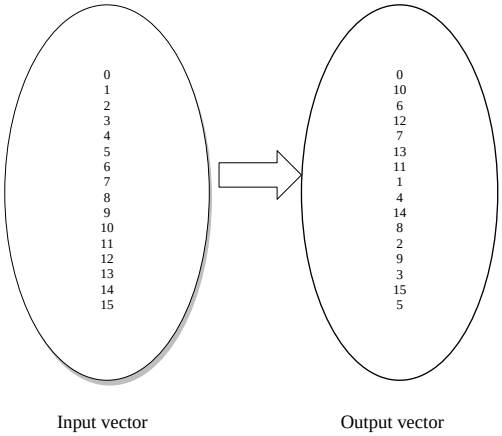
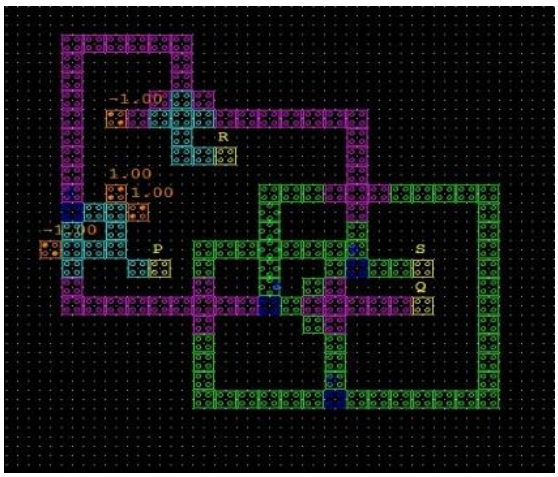
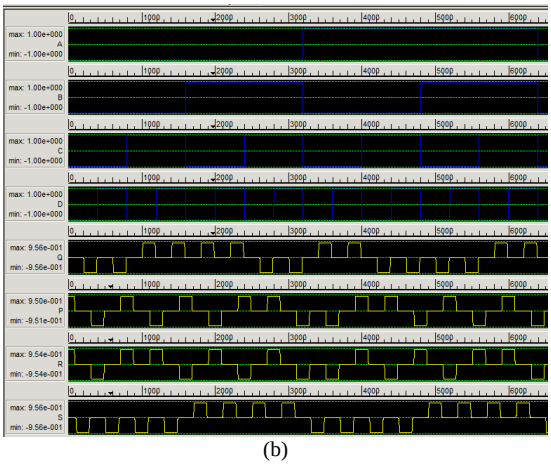


Fig.6. Bijective nature of proposed logic

For the verification of the truth table QCADesigner 2.0.3 is taken in consideration and schematic as well as waveform is shown in fig.7.



(a)



(b)

Fig.7. SA Logic (a) schematic (b) waveform on QCA

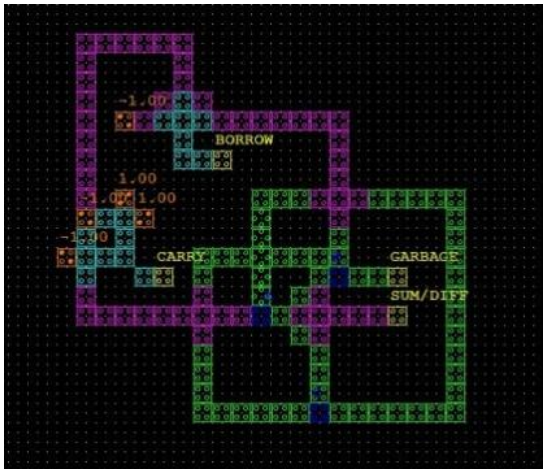
Using this logic various combinational circuits like adder and subtractor can be designed. On treating D as constant input of 0 we can obtain full adder/subtractor circuit while on setting both C and D to a constant input of 0 we can obtain Half Adder /Subtractor circuit.

A. SA Logic as Full adder/Subtractor:

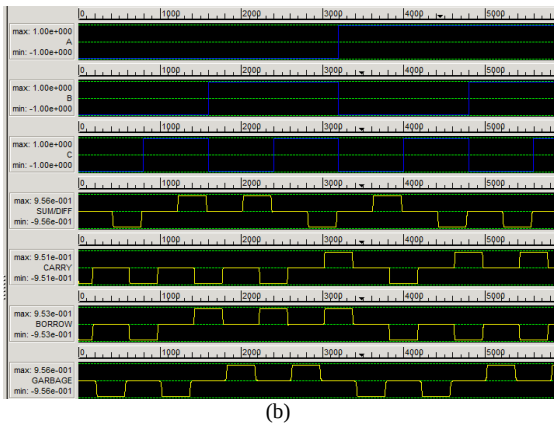
Full adder/ Subtractor are a combinational circuit performing addition/ subtraction for 3 inputs (A, B, C) and generating output as Sum/Diff, Carry and borrow; Table 4 shows its truth table. The full adder/subtractor can be implemented using the proposed SA logic if the fourth input bit i.e. D is set to 0 resulting in 3 inputs(A, B, C) , 3 outputs(sum/diff, carry, borrow) and 1 garbage bit. The QCA layout and waveform is shown in fig.8.

Table 4. Truth Table of FA/FS

A	B	C	Sum/ Diff	Carry	Borrow
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	1	1	1



(a)



(b)

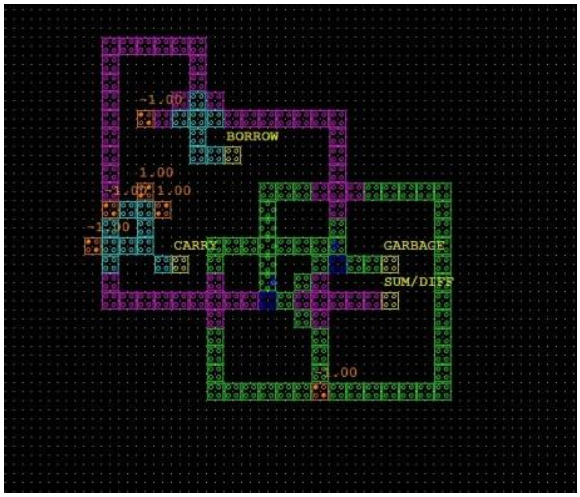
Fig.8. SA logic as Full adder/ subtractor (a)schematic (b) waveform on QCA

B. SA Logic as Half adder/Subtractor:

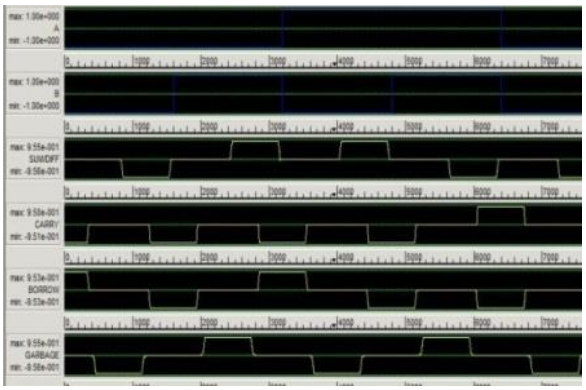
Half adder/ Subtractor is a combinational circuit performing addition/ subtraction for 2 inputs (A, B) and generating output as Sum/Diff, Carry and borrow shown in table 5. In the proposed logic if third and fourth bit are set to zero value then it will act as a half adder/subtractor circuit consisting of 2 inputs(A, B), 3 outputs(sum/diff, carry, borrow) and 1 garbage outputs depicted in fig.9

Table 5. Truth Table of HA/HS

A	B	Sum/ Diff	Carry	Borrow
0	0	0	0	0
0	1	1	0	1
1	0	1	0	0
1	1	0	1	0



(a)



(b)

Fig.9. SA logic as Half Adder/Subtractor (a)schematic (b) waveform on QCA

V. Results and Discussion

For the sake of verifying the proposed circuits some of the parameters have been taken in consideration shown in fig.10. These are by-default criterion in QCADesigner [10]. The proposed circuit has been designed in single layer and consists of coplanar wire crossing. Its effective area is 0.17 μm^2 consisting of 137 cells.

Table 6. Comparative Analysis of Reversible Full Adder/ Subtractor Circuit

	No. of Gates Used	No. of garbage Output	No. of Constant Input	Circuits Formed	Tool Used
Design 1 [13]	8	5	3	1(Full Adder)	Xilinx
Design 2 [13]	4	3	1	1(Full Adder)	Xilinx
Design 3 [13]	4	3	1	1(Full Adder)	Xilinx
Fredkin Gate [14]	6	5	4	1(Full Adder)	-
DKG Gate [15]	1	2	1	2(Full Adder, Full Subtractor)	Xilinx
TSG Gate [16]	1	2	1	1(Full Adder)	Tanner
OTG Gate [17]	1	2	1	1(Full Adder)	-
Inventive0 Gate [18]	1	2	1	2(Full Adder, Full subtractor)	Microwind DSH-2.7
DG[19]	2	2	1	1(Full Aubtractor)	QCA
TG[20]	2	2	1	1(Full Subtractor)	-
Feynman and Peres gate[21]	4	3	1	2(Full Adder, Full Subtractor)	-
Peres Gate[22]	2	2	1	1(Full Adder)	Tanner EDA with TSMC018 Technology
Peres Gate[23]	2	2	1	1(Full Adder)	Xilinx ISE
IG Gate[24]	2	2	2	1(Full Adder)	-
New , toffoli, Feynman gate[25]	3	3	1	1(Full Adder)	-
Fredkin gate[26]	4	3	2	1(Full Adder)	-
Proposed Design	1	2	1	2(Full Adder, Full Subtractor)	QCA

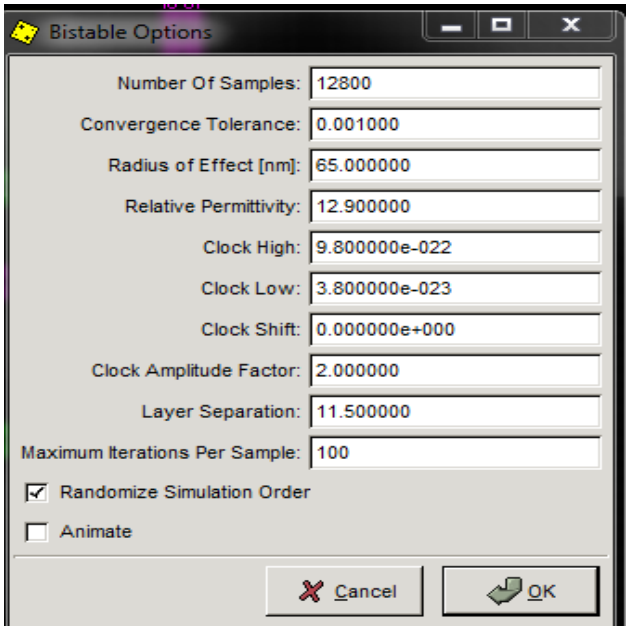


Fig.10. QCADesigner Parameters

Energy dissipation can be calculated using QCA Designer–E [11] on considering parameters shown in fig.11.

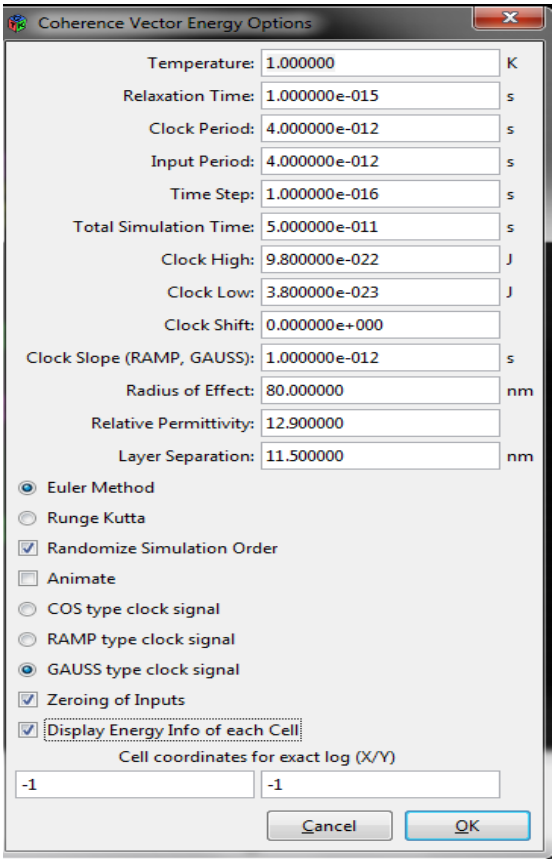


Fig.11. QCADesigner-E coherence vector energy option

QCADesigner-E is actually simulation module of QCA Designer, the parameter description can be seen from data sheet [12]. The simulation result display on enabling the option of display energy info of each cell in the coherence vector simulation as shown below:

Sum_bath: S_b 7.98e-002

S_{bE} -7.72e-003

Avg_bath: A_b 7.25e-003

A_{bE} -7.02e-004

Sum_clk: S_c -1.29e-002,

Avg_clk: A_c -1.18e-003

Comparative Analysis:

After a rigorous review of various papers comparative analysis of the proposed Full Adder/Subtractor design with some of the existing ones is enlisted in Table 6. This table demonstrates that the proposed design is capable of implementing reversible full adder/subtractor circuit on QCA using single gate, minimal garbage output as well as constant input.

VI. Conclusion

This paper presents a QCA layout of SA logic, applicable in designing of various combinational circuits like half adder, full adder, half subtractor and full subtractor with minimal garbage output. The simulation result confirms the operation of the design using the ideal bi-stable options. This, design can be a good move in the combinational circuits design. The proposed SA logic can be used in application of ALU designing for arithmetic operations as well as it can be used in bus interface unit i.e. for physical address generation etc.

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Authors' Profiles

Er. Snigdha Singh received her B. Tech. degree in Electronics and Communication Engineering in 2014 and currently pursuing her M. Tech. degree in Microelectronics Engineering at Institute of Engineering and Technology, Lucknow. Her research interests are in area of the field of high speed nanotechnology, Quantum Dots and VLSI design.

Er. Abhinay Choudhary received his B. Tech. degree in Electronics and Communication Engineering in 2016 and currently pursuing his M. Tech. degree in Microelectronics Engineering at Institute of Engineering and Technology, Lucknow. His research interests are in area of the field of high speed nanotechnology, Quantum Dots and VLSI design.

Manoj Kumar Jain received his B.E. degree in Electronics Engineering in 1994, M. Tech. degree in Electronics and Communication Engineering in 2011 and Ph. D. degree Electronics Engineering in 2017. His research work and interest are focused on microelectronics, analog integrated circuits, analog signal processing and VLSI design.

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