

# Temporal Logics Specifications for Debit and Credit Transactions

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Abstract— Recently, with the emergence of mobile technology and mobile banking, debit and credit transactions have been the most common transactions that are widely spreading, using such technologies. In this research, we specify the concurrent debit and credit transactions in temporal logics such as CTL (Computational Tree Logic) and LTL (Linear-Time Temporal Logic). These specifications describe the infinite histories that may be produced by the iterations of such concurrent transactions infinitely many times. We represent the infinite histories as a model of temporal logics formulae. Then, model checkers, such as NuSMV or SPIN, can carry out exhaustive checks of the correctness of the concurrent debit and credit transactions. Moreover, in this paper, we presume that the serializability condition is too strict. Therefore, a relaxed condition has been suggested to keep the database consistent. Moreover, the relaxed condition is easier to encode into temporal logics formulae.

*Index Terms*— Debit And Credit Transactions, Temporal Logics Specifications, Model Checking, Serializability of Transactions.

## I. INTRODUCTION

In recent times, temporal logic stands out as one of the tools that is useful to specify and reason about concurrent and reactive systems because it provides a natural way to describe the temporal behavior of these kinds of systems [1]. It is possible to represent the systems and their properties by using temporal logics formulae. Also, we can express the implementations and specifications of the system as two formulae written using temporal logics, and then, verify whether the implementations imply the specifications. Modern operating systems and most of DBMS's extensively make use of concurrent algorithms [2], [3]. Hence, the correctness of these algorithms is very important to achieve system reliability. Now, the wide use of mobile and banking technologies has led to a huge number of concurrent users, may be, processing their database transactions simultaneously. In this case, infinite histories will be produced. The importance of representing such infinite histories has been considered [4], [5] and [6]. Usually, database techniques deal with a finite number of transactions concurrently executing [7] and [8].

Our research issue, in this paper, is to specify an infinite history of the debit and credit transactions in term of serializability, as a correctness criterion, using temporal logics formulae. The availability of model checkers gives importance to the temporal logics specifications. In this context, model checkers can carry out exhaustive checks for a correctness criterion of concurrent debit and credit transactions automatically with no need to the expertise in carrying out the verification [9] and [10].

Some researchers, in general, have taken into their accounts representing infinite histories in temporal logics [11] and [12]. And, they presumed that the serailizability is the correctness condition. In this research, we will introduce a computationally efficient condition of serializability that can be used to specify the correctness of concurrent transactions in temporal logics such as CTL and LTL. The serializability condition is relaxed in a way that keeps database in a consistent state. This condition is based on the nature of debit and credit transactions.

This paper is organized as follows. In Section II, we shall discuss the debit and credit transactions, conflict serializability condition and the relaxed condition of serializability. The syntaxes and the semantics of LTL and CTL are introduced in Section III . In Section IV, the properties of transition structure for read and write operations and their interpretations on LTL and CTL paths are depicted. Furthermore, The encoding of debit and credit transactions into LTL and CTL and the relaxed serializability condition are also given in Section IV. The conclusions are drawn in Section V.

## II. DEBIT AND CREDIT TRANSACTIONS MODEL

## A. Debit and Credit Transactions Model

In general, transaction is a collection of one or more operations on one or more databases. Formally as in [9], [4], [11] and [12], a transaction is a sequence of read/write operations partially ordered such that:

A transaction  $T_i$  is a partial order with ordering relation  $\leq_i$ , such that if  $r_i(x), w_i(x) \in T_i$  then either  $r_i(x) \leq_i w_i(x)$  or  $w_i(x) \leq_i r_i(x) \quad \forall x.x \in D = \{x_1, x_2, \dots, x_m\}$ . In this paper, we shall denote to the set of data items that are accessed by all transactions by D.

## **Definition 1**:

A debit or credit transaction  $T_i$ , accesses a set of data items  $D_i = \{x_1, x_2, ..., x_k\} \subseteq D$ , is a sequence of (totally ordered) of read and write operations, where every read operation  $r_i(x)$  precedes write operation  $w_i(x), \forall x.x \in D_i$ , such that

$$T_i = r_i(x_1) w_i(x_1) \dots r_i(x_k) w_i(x_k)$$

As in [11],[9] and [13], a set of debit and credit transactions is denoted by  $T = \{T_i : i = 1, 2, ...\}$ . A history h is an interleaving sequence of read and write operations belonging to different transactions in T. Hence, a transaction  $T_i \in T$  participating, in a history h, is a subsequence of operations where every read and write operations occurring in a history h in the same order as they do in  $T_i$ . We shall denote to the operation  $O_i$  (where  $O_i$  is a read or write operation in a transaction  $T_i$  ) occurs in a history h before operation  $o_i$  by  $o_i <_h o_j$ . In this paper, we assume that history h is considered to be serializable or correct (preserve the database in a consistence state) if it is equivalent to a serial execution of all transactions in T [14]. We formally define that two histories are equivalent as follows:

## **Definition 2**:

Histories  $h_1$  and  $h_2$  of  $T = \{ T_i : i = 1, 2, .. \}$  are equivalent, written as  $h_1 \sim h_2$ , iff for all  $i_1, i_2 \ge 1, i_1 \ne i_2$ , and for all  $x \in D$ ,

$$\begin{aligned} &I) \ If \ r_{i_{1}}\left(x\right) <_{h_{1}} w_{i_{2}}(x), \ then \ r_{i_{1}}\left(x\right) <_{h_{2}} w_{i_{2}}(x), \\ &2) \ If \ w_{i_{1}}\left(x\right) <_{h_{1}} w_{i_{2}}(x), \ then \ w_{i_{1}}\left(x\right) <_{h_{2}} w_{i_{2}}(x) \ and \\ &3) \ If \ w_{i_{1}}\left(x\right) <_{h_{1}} r_{i_{2}}(x), \ then \ w_{i_{1}}\left(x\right) <_{h_{2}} r_{i_{2}}(x). \end{aligned}$$

We say that the history h is serializable if h is equivalent to a serial history  $h_s$ , as in the next definition.

## **Definition 3**:

A history h of  $T = \{ T_i : i = 1, 2, ... \}$  is serializable iff there is a serial history  $h_s$  of T of the form, for each i = 1, 2, ...,

$$h_S = \dots \underbrace{\dots r_i(x) \dots w_i(y)}_{\text{only (all) steps of } T_i} \dots$$

such that  $h \sim h_s$ .

## B. Conflict graph and serilizability

Conflict graph is a directed graph that is built and used to test whether a history h, of the concurrent transactions, is serializable, and subsequently is a correct history. We consider that the history h is serializable if there is no

cycle in the corresponding conflict graph. The importance of this graph is that the test of serializability can be done in a polynomial time [14]. We shall consider that two operations are conflicting, if belonging to different transactions, accessing the same data item and one of them is a write operation. Next, we shall define how we can build a conflict graph of concurrent transactions participating in a history h.

## **Definition 4**:

For each history h, there is a directed graph CG(h)called the conflict graph of h. This graph has the transactions of h as its nodes, and contains an arc  $(T_{i_1}, T_{i_2})$ , where  $T_{i_1}$  and  $T_{i_2}$  are distinct transactions of h, whenever there is a operation of  $T_{i_1}$  which conflicts with a subsequent (in h) operation of  $T_{i_2}$ .

## C. Serilizability of Debit and Credit Transactions

Usually, bank customers are interacting with bank database by invoking debit and credit transactions. Debit and credit transactions are representing the deposit and withdrawal to and from current balance of a bank account [15]. So, to understand the serializability of debit and credit transactions that are concurrently executing in a database, we shall give the following example:

Suppose that we have two data items x and y which are representing two bank accounts in a bank database, two transactions such that:

$$T_{1}:r_{1}(x); x = x - 100; w_{1}(x); r_{1}(y); y = y + 100; w_{1}(y)$$

$$T_{2}:r_{2}(y); y = y - 200; w_{2}(y); r_{2}(x); x = x + 200; w_{2}(x)$$

and assume that the concurrent execution of the transactions as follows:

$$h = r_1(x)w_1(x)r_2(y)w_2(y)r_1(y)w_1(y)r_2(x)w_2(x).$$

Now, suppose the initial value of x is 1000 (x = 1000) and the initial value of y is 500 (y = 500). After execution above the history h, the final values of x and y are 1100 and 400, respectively. But, the serializable execution of the two transactions  $T_1$  and  $T_2$  is such that:

$$h_{s} = r_{1}(x)w_{1}(x)r_{1}(y)w_{1}(y)r_{2}(y)w_{2}(y)r_{2}(x)w_{2}(x).$$

Suppose that we have that the same initial values for x and y (x = 1000, y = 500), then the final values of x and y, after execution of the history  $h_s$ , are 1100 and 400, respectively. This means that the final values of the concurrent transactions in the history h is correct.

But, according to the **Definition 2** and **Definition 3**, h is not seilaizable because it is not equivalent to the serial history  $h_s$  ( $h - h_s$ ) and does not leave the database in a consistent state. Moreover, if we build the conflict graph that is corresponding to the history h as in Fig. 1, then we notice that the graph contains a cycle. This means that the history h is not serializable and subsequently it is not a correct history.



Fig. 1. Conflict graph of the history h.

Now, the above demonstration shows that the history h is not serializable but, at the same time, it is correct. The reason is that the addition and subtraction operations that are applied on debit and credit transactions are commutative and can be applied in any order [15]. This means that the condition of serializability in **Definition 2** and **Definition 3** is too restrictive. So, the relaxed condition of serializability of debit and credit transactions is defined formally as follows:

## **Definition 5**:

A history hr of debit and credit transactions  $T = \{T_i : i = 1, 2, ...\}$  is serializable iff, for any transaction  $T_i \in T$  and data item  $x \in D$ , the read and write  $(r_i(x) \text{ and } w_i(x))$  are occurring in the history hr without interleaving with any other operation(s) from different transactions  $T_j \in T$  of the same data item x. This will be of the form, for each i = 1, 2, ...

$$hr = \dots \underbrace{r_i(x) \dots w_i(x)}_{\text{no } r_i(x) \text{ or } w_i(x)}$$

To demonstrate the above definition, consider the transactions that are in the above example such that

$$T_{1}:r_{1}(x); x = x - 100; w_{1}(x); r_{1}(y); y = y + 100; w_{1}(y)$$

$$T_{2}:r_{2}(y); y = y - 200; w_{2}(y); r_{2}(x); x = x + 200; w_{2}(x)$$

and the following history

$$h_d = r_1(x)r_2(y)w_2(y)w_1(x)r_1(y)w_1(y)r_2(x)w_2(x).$$

Now, suppose that we have that the same initial values for x and y (x = 1000, y = 500) as in the above example, then the final values of x and y, after execution of the history  $h_d$ , are 1100 and 400, respectively. This means that the final values of the concurrent transactions in the history  $h_d$  are correct. Moreover, the **Definition 5** allows the operations from different transactions which are accessing different data items to be interleaved. This will relax the serializability condition in **Definition 2** and **Definition 3** to a new one which can be encoded into temporal logics in an easier way as we shall see later in this paper.

## D. Infinite History of Debit and Credit Transactions

For the last decade, most people around the world have had smart mobile phones. Accordingly, a huge number of people access the Internet for shopping. Bank transactions involve deposit and withdraw to/form bank accounts. These are called debit and credit transactions. In 2015, the expectations say that over 900 million people are expected to transact \$1 trillion in the global mobile market [16]. So, we can expect that the number of debit and credit transactions is huge and the transactions are non-stopping. This means that millions of people are constantly depositing and withdrawing to/from bank accounts. Also, the statistics show that the use of mobile transactions for debit and credit in the developing countries has excessively increased, see Fig. 2. Such situation will produce infinite histories of debit and credit transactions.

Most database management systems consider that the histories are finite but such applications signify the need to deal with infinite histories [17]. One of the most techniques that can deal with modeling of infinite and finite behavior is temporal logics [18]. These histories will be encoded in temporal logics formulae as we will see in the next sections.



Source: Bain/Research Now and Bain/ GMI NPS Surveys, 2013. Fig. 2 Mobile Payment in 2013.

## **III. TEMPORAL LOGICS**

In this section, we will introduce two famous types of temporal logics: Linear-Time Temporal Logic (LTL) and Computational Tree Logic (CTL).

## A. LTL Syntax and Semantics

LTL is a logic that can be used to specify infinite histories composed of *n* transactions repeating infinitely many times. The compilation of all the iterations of the *n* transactions gives an infinite number of transactions  $T = \{T_i : i = 1, 2, ...\}$ . The reason for using LTL as a specification language is that the LTL formulae can be interpreted over infinite sequence of states which are useful for the histories that are produced in this context [19], [20]. Furthermore, LTL is accepted as a specification language in modern model checkers such as NuSMV.

## B. Syntax of LTL

The alphabet of LTL consists of a set of propositions symbols  $p_i, i = 0, 1, 2, ...,$  read/write step propositional symbols  $r_i(x_j), w_i(x_j)$ , where  $i \ge 1$  and  $1 \le j \le |D|$ , boolean operations  $\neg, \lor, \land, \bullet, \bot$ , and temporal operators **X**, **F**, **G**, **U**. Formulae in LTL are of the form:

$$\phi ::= p_i | r_i(x_j) | w_i(x_j) | \neg \phi | \phi_1 \lor \phi_2 | \phi_1 \land \phi_2 | \mathbf{X} \phi |$$
$$\mathbf{F} \phi | \mathbf{G} \phi | \phi_1 \mathbf{U} \phi_2.$$

The symbols  $\perp$  and  $\bullet$  denote the truth values false and true respectively and the abbreviations  $\Rightarrow$  and  $\Leftrightarrow$ will denote usual implication and equivalency in logic, respectively.

## C. Semantics of LTL

An interpretation for LTL,  $I(s_i)$ , at a given state  $s_i \in S$ , where S is a set of states, assigns truth values  $p_j^{I(s_i)}$ ,  $r_i(x_j)^{I(s_i)}$  and  $w_i(x_j)^{I(s_i)}$  ( $\in \{\perp, \bullet\}$ ) to propositional symbol  $p_j$ ,  $r_i(x_j)$  and  $w_i(x_j)$ , respectively. The model M, of the system to be specified, is represented by a structure of transition system called kripke structure see [4]. The *semantics* of a LTL formula  $\phi$  is interpreted by the truth relation  $M, s_i ` \phi$  which means that  $\phi$  holds at state  $s_i$  in the model structure M. If  $\phi$  is a path formula,  $M, \pi ` \phi$  means that  $\phi$  holds along path  $\pi$  in the Kripke structure M. The relation ` is defined as follows:

$$M, s_i ` p_j \text{ iff } p_j^{I(s_i)} = \bullet$$

$$M, s_i ` r_i(x_j) \text{ iff } r_i(x_j)^{I(s_i)} = \bullet$$

$$M, s_i ` w_i(x_j) \text{ iff } w_i(x_j)^{I(s_i)} = \bullet$$

$$M, s_i ` \neg \phi \text{ iff } M, s_i - \phi$$

$$M, s_i ` \phi_1 \lor \phi_2 \text{ iff } M, s_i ` \phi_1 \text{ or } M, s_i ` \phi_2$$

$$M, s_i ` \phi_1 \land \phi_2 \text{ iff } M, s_i ` \phi_1 \text{ and } M, s_i ` \phi_2$$

$$M, s_i ` \mathbf{X}\phi \text{ iff } M, s_{i+1} ` \phi$$

$$M, s_i ` \mathbf{F}\phi \text{ iff there exists } k \ge i \text{ such there}$$

 $M, s_i \in \mathbf{F}\phi$  iff there exists  $k \ge i$  such that  $M, s_k \in \phi$ 

$$M, s_i ` \mathbf{G}\phi$$
 iff for all  $k \ge i$  such that  $M, s_k ` \phi$   
 $M, s_i ` \phi_1 \mathbf{U}\phi_2$  iff there exists  $c \ge i$ ,  $M, s_c ` \phi_2$ 

and, for all  $i \le b < c, M, s_b$  '  $\phi_1$ .

## D. CTL syntax and semantics

Actually, LTL and CTL formulae are different in their interpretations. Therefore, some formulae in LTL cannot be specified in the CTL formulae and vice versa. LTL formula is considering each path isolated. Hence, if each individual path holds the path formula, then LTL formula is true. But, To interpret a CTL formula, we consider the alternative possibilities for each state in a path.

## E. CTL syntax

As in Subsection *B*, the alphabet of *CTL* consists of a set of propositions symbol  $p_0, p_1, \ldots$ , read/write step propositional symbols  $r_i(x_j), w_i(x_j)$   $(1 \ge 1, 1 \le j \le |D|)$ , boolean operations  $\neg, \lor, \land, \bullet, \bot$ , quantifiers **E**, **A**, temporal operators **X**, **F**, **G** and **U**. Formulae in *CTL* are generated by:

$$\phi ::= p_i | r_i(x_j) | w_i(x_j) | \neg \phi | \phi_1 \lor \phi_2 | \phi_1 \land \phi_2 | \mathbf{A} \mathbf{X} \phi$$
$$\mathbf{E} \mathbf{X} \phi | \mathbf{A} \mathbf{F} \phi | \mathbf{E} \mathbf{F} \phi | \mathbf{A} \mathbf{G} \phi | \mathbf{E} \mathbf{G} \phi | \mathbf{A} [\phi_1 \mathbf{U} \phi_2]$$
$$\mathbf{E} [\phi_1 \mathbf{U} \phi_2].$$

In this logic,  $r_i(x_j)$  and  $w_i(x_j)$  are propositions but not predicates. The symbols  $\perp$ , • ,  $\Rightarrow$  and  $\Leftrightarrow$  have the same logical meaning as in Subsection *B*.

## F. Semantics of CTL

In this subsection, we shall use the same interpretation function  $I(s_i)$  with the same meaning which has been introduced in Subsection *C*. in addition, the set of paths starting in a state  $s_i$  is denoted  $Paths(s_i)$  with  $Paths(s_i) \neq \{\}$ . Therefore, the relation ' is defined inductively as follows:

$$M, s_{i} ` p_{j} \text{ iff } p_{j}^{I(s_{i})} =? .$$

$$M, s_{i} ` r_{i}(x_{j}) \text{ iff } r_{i}(x_{j})^{I(s_{i})} =\bullet .$$

$$M, s_{i} ` w_{i}(x_{j}) \text{ iff } w_{i}(x_{j})^{I(s_{i})} =\bullet .$$

$$M, s_{i} ` \neg \phi \text{ iff } M, s_{i} -\phi .$$

$$M, s_{i} ` \phi_{1} \lor \phi_{2} \text{ iff } M, s_{i} ` \phi_{1} \text{ or } M, s_{i} ` \phi_{2} .$$

$$M, s_{i} ` \phi_{1} \land \phi_{2} \text{ iff } M, s_{i} ` \phi_{1} \text{ and } M, s_{i} ` \phi_{2} .$$

$$M, s_{i} ` \mathbf{AX} \phi \qquad \text{iff, for all}$$

$$\pi \in Paths(s_{i}), M, s_{i+1} ` \phi$$

 $M, s_i \in \mathbf{EX}\phi$  iff there exists  $\pi \in Paths(s_i)$  such that  $M, s_{i+1} \notin \phi$ .

 $M, s_i$  '  $\mathbf{AF}\phi$  iff, for all  $\pi \in Paths(s_i)$ , there exists  $b \ge i$  such that  $M, s_h$  '  $\phi$ .

 $M, s_i$  ' **EF** $\phi$  iff there exists  $\pi \in Paths(s_i)$  and  $b \ge i$  such that  $M, s_h$  '  $\phi$ .

 $M, s_i$  '  $\mathbf{AG}\phi$  iff, for all  $\pi \in Paths(s_a)$ , and, for all,  $b \ge i, M, s_b$  '  $\phi$ .

 $M, s_i$  ' **EG** $\phi$  iff there exists  $\pi \in Paths(s_i)$  such that, for all  $b \ge i, M, s_b$  '  $\phi$ .

 $M, s_i ` \mathbf{A}[\phi_1 \mathbf{U}\phi_2]$  iff, for all  $\pi \in Paths(s_i)$ , there is some  $c \ge i$  such that  $M, s_c ` \phi_2$  and, for all  $a \le b < c, M, s_b ` \phi_1$ .

 $M, s_i \in \mathbf{E}[\phi_1 \mathbf{U}\phi_2]$  iff there exists  $\pi \in Paths(s_i)$ such that, for some  $c \ge i, M, s_c \in \phi_2$  and, for all  $i \le b < c, M, s_b \in \phi_1$ .

## IV. ENCODING DEBIT AND CREDIT TRANSACTIONS INTO LTL AND CTL

In this section, we shall give transition structure that has, at each state, a set of propositions which are either true or false. Therefore, as in [4], the set of propositions for each debit and credit transaction should satisfy the following properties:

## (C1) Write implies read

A transaction  $T_i$  can only be written to  $x_i$  if it has read

 $x_j$ , i.e. if  $w_i(x_j)$  executes, then  $r_i(x_j)$  must have been executed before.

## (C2) Read/write step proposition remains

## true until the transaction ends

If a read/write step has taken place, the corresponding proposition remains true until the transaction ends, i.e.  $r_i(x_j)/w_i(x_j)$  is true, remains true until all operations belonging to the same transactions become true.

(C3) At most one step occurs at each

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successive state
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No two or more distinct steps can be false in a state, and then become true in a next state.

(C4) Each read operation  $r_i(x_j)$  should precede a write operation  $w_i(x_j)$  without existence of any other read/write

operation separate them.

This property emphasizes that the transaction of the form

$$T_i = r_i(x_1) w_i(x_1) \dots r_i(x_k) w_i(x_k)$$

as in *Definition 1*.

The *semantics* of the temporal formula (in CTL or LTL)  $\phi$  is given by a truth relation  $M, s_i \circ \phi$ , where M is a

structure that satisfies the additional conditions (C1)-(C4). Therefore, given a state  $s_i$ , and a path  $\pi \in Paths(s_i)$ , there corresponds a sequence of read and write step propositions that become true in  $s_i, s_{i+1}, \ldots$ . In this way,  $\pi$  yields a history of infinitely many occurrences (iterations) of the transactions  $T_1, \ldots, T_n$  which are composing  $T = \{T_i : i = 1, 2, \ldots\}$ .

We illustrate this correspondence between paths and histories by the following example:

Assume that we have the set of data items  $D = \{x, y\}$ and the debit and credit transactions are

$$T_1 = r_1(x)w_1(x)r_1(y)w_1(y) \text{ and}$$
  

$$T_2 = r_2(y)w_2(y)r_2(x)w_2(x).$$

The truth and the falsity for each read and write step propositions are given for successive states, and the top of each column, in Fig. 3, represents the unique proposition that becomes true in that state. The corresponding history h is:

$$h = r_1(x)r_2(y)w_2(y)w_1(x)r_1(y)w_1(y)r_2(x)w_2(x).$$

$r_1(x)$	$r_2(y)$	$w_2(y)$	$w_1(x)$	$r_1(y)$
<i>s</i> <sub>0</sub>	$S_1$	<i>s</i> <sub>2</sub>	<i>S</i> <sub>3</sub>	$s_4$
•	•	•	•	•
$r_1(x)$	$r_1(x)$	$r_1(x)$	$r_1(x)$	$r_1(x)$
$\neg w_1(x)$	$\neg w_1(x)$	$\neg w_1(x)$	$w_1(x)$	$w_1(x)$
$\neg r_1(y)$	$\neg r_1(y)$	$\neg r_1(y)$	$\neg r_1(y)$	$r_1(y)$
$\neg w_1(y)$	$\neg w_1(y)$	$\neg w_1(y)$	$\neg w_1(y)$	$\neg w_1(y)$
$\neg r_2(y)$	$r_2(y)$	$r_2(y)$	$r_2(y)$	$r_2(y)$
$\neg w_2(y)$	$\neg w_2(y)$	$w_2(y)$	$w_2(y)$	$w_2(y)$
$\neg r_2(x)$	$\neg r_2(x)$	$\neg r_2(x)$	$\neg r_2(x)$	$\neg r_2(x)$
$\neg w_2(x)$	$\neg w_2(x)$	$\neg w_2(x)$	$\neg w_2(x)$	$\neg w_2(x)$

$w_1(y)$	$r_2(x)$	$w_2(x)$	
<i>S</i> <sub>5</sub>	<i>s</i> <sub>6</sub>	<i>S</i> <sub>7</sub>	∞
•	•	•	
$r_1(x)$	$r_1(x)$	$r_1(x)$	
$w_1(x)$	$w_1(x)$	$w_1(x)$	
$r_1(y)$	$r_1(y)$	$r_1(y)$	
$w_1(y)$	$w_1(y)$	$w_1(y)$	∞

$r_2(y)$	$r_2(y)$	$r_2(y)$
$w_2(y)$	$w_2(y)$	$w_2(y)$
$\neg r_2(x)$	$r_2(x)$	$r_2(x)$
$\neg w_2(x)$	$\neg w_2(x)$	$w_2(x)$

Fig. 3. The correspondence between path and history

#### A. CTL and LTL Specifications

Now, the transactions model properties (or conditions) (C1)-(C4) can be encoded as follows

## (C1) Write implies read

A transaction  $T_i$  can only be written to  $x_i$  if it has read

 $x_j$ , i.e. if  $w_i(x_j)$  executes, then  $r_i(x_j)$  must have been executed before.

1. CTL specification is:

$$\sigma_{1} = \bigwedge_{1 \le i \le n} \bigwedge_{1 \le j \le m} \operatorname{AG}(w_{i}(x_{j}) \Longrightarrow r_{i}(x_{j})) \tag{1}$$

2. LTL specification is:

$$\sigma_{1}' = \bigwedge_{1 \le i \le n} \bigwedge_{1 \le j \le m} \mathbf{G}(w_{i}(x_{j}) \Longrightarrow r_{i}(x_{j}))$$
(2)

We shall add an extra proposition called  $end_i$  to indicate that the occurrence of  $T_i$  ends. This can be specified in CTL as follows

$$\sigma_0 = \bigwedge_{1 \le i \le n} \mathbf{AG}(end_i \Leftrightarrow \bigwedge_{1 \le j \le m} (r_i(x_j) \land w_i(x_j)))$$
(3)

also,  $\sigma_0$  can be substituted in LTL by

$$\sigma'_{0} = \bigwedge_{1 \le i \le n} \mathbf{G}(end_{i} \Leftrightarrow \bigwedge_{1 \le j \le m} (r_{i}(x_{j}) \land w_{i}(x_{j}))) \quad (4)$$

## (C2) Read / write step proposition remains

## true until the transaction ends

If a read/write step has taken place, the corresponding proposition remains true until the transaction ends, i.e.  $r_i(x_j) / w_i(x_j)$  is true, remains true until all operations belonging to the same transactions become true.

1. CTL specification is:

$$\sigma_{2} = \bigwedge_{\substack{1 \le i \le n \\ 1 \le j \le m}} \mathbf{AG}((r_{i}(x_{j}) \land \neg end_{i} \Rightarrow \mathbf{AX}r_{i}(x_{j})))$$

$$\wedge (w_{i}(x_{j}) \land \neg end_{i} \Rightarrow \mathbf{AX}w_{i}(x_{j})))$$
(5)

2. LTL specification is:

$$\sigma_{2}' = \bigwedge_{\substack{1 \le i \le n \\ 1 \le j \le m}} \mathbf{G}((r_{i}(x_{j}) \land \neg end_{i} \Rightarrow \mathbf{X}r_{i}(x_{j})))$$

$$\wedge (w_{i}(x_{i}) \land \neg end_{i} \Rightarrow \mathbf{X}w_{i}(x_{i})))$$
(6)

## (C3) At most one step occurs at each

## successive state

No two or more distinct steps can be false in a state, and then become true in a next state.

1. CTL specification is:

$$\sigma_{3} = \bigwedge_{\substack{1 \leq i, i' \leq n \\ 1 \leq j, j' \leq m \\ i \neq i' \text{ or } j \neq j'}} \mathbf{AG}[\neg((\neg r_{i}(x_{j}) \land \neg r_{i'}(x_{j'}))) \land \mathbf{EX}(r_{i}(x_{j}) \land \neg r_{i'}(x_{j'}))) \land (\neg r_{i}(x_{j}) \land \neg w_{i'}(x_{j'}))) \land \mathbf{EX}(r_{i}(x_{i}) \land w_{i'}(x_{j'}))) \land (\neg w_{i}(x_{j}) \land \neg w_{i'}(x_{j'}))) \land \mathbf{EX}(r_{i}(x_{j}) \land \neg w_{i'}(x_{j'}))) \land \mathbf{EX}(w_{i}(x_{j}) \land \neg w_{i'}(x_{j'})))].$$

$$(7)$$

2. LTL specification is:

In the CTL specification in (7) we use the operators AGEX. Likewise, there is no LTL specification that is equivalent to the CTL specification. So, we can say that, there are properties that can be expressed in CTL but cannot be expressed in LTL and vice versa.

(C4) Each read operation  $r_i(x_j)$  should precede a write operation  $w_i(x_j)$  without existence of any other read/write operation separate them.

1. CTL specification is:

$$\sigma_4 = \bigwedge_{1 \le i \le n} \bigwedge_{1 \le j \ne j' \le m} \neg \mathbf{EF}(r_i(x_j) \land r_i(x_{j'}) \land \neg w_i(x_j) \land \neg w_i(x_j))$$

$$\land \neg w_i(x_{j'}))$$
(8)

2. LTL specification is:

$$\sigma_{4}' = \bigwedge_{1 \le i \le n} \bigwedge_{1 \le j \ne j' \le m} \neg \mathbf{F}(r_{i}(x_{j}) \land r_{i}(x_{j'}) \land \neg w_{i}(x_{j}) \land \neg w_{i}(x_{j'})) \land \neg w_{i}(x_{j'})).$$
(9)

Now, to make sure that all read and write operations do not become true after the transaction  $T_i$  ends, we shall add the following specification:

$$\sigma_{5} = \bigwedge_{1 \le i \le n} \mathbf{AG}(end_{i} \Rightarrow \mathbf{AX}(\bigwedge_{1 \le j \le m} (\neg r_{i}(x_{j}) \land \neg w_{i}(x_{j}))) \land \neg end_{i})).$$
(10)

or

$$\sigma'_{5} = \bigwedge_{1 \le i \le n} \mathbf{G}(end_{i} \Rightarrow \mathbf{X}(\bigwedge_{1 \le j \le m} (\neg r_{i}(x_{j}) \land \neg w_{i}(x_{j})))$$

$$(11)$$

$$(11)$$

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I.J. Information Technology and Computer Science, 2015, 05, 10-17

We denote by  $\sigma_{dct}$  (as in (12)) the specification that the transition structure of the histories (of debit and credit transactions) should satisfy. i.e

$$\sigma_{dct} = (\sigma_0 \lor \sigma'_0) \land (\sigma_1 \lor \sigma'_1) \land (\sigma_2 \lor \sigma'_2) \land \sigma_3 \land (\sigma_4 \lor \sigma'_4) \land (\sigma_5 \lor \sigma'_5).$$
(12)

Next, we shall encode the relaxed condition of serializability for Debit and Credit transaction (see *Definition 5*)

$$\sigma_{rcs} = \bigwedge_{1 \le i \le n} \bigwedge_{1 \le j \ne i \le n} \operatorname{AG}(r_i(x_k) \land r_j(x_k))$$

$$\Rightarrow (w_i(x_k) \lor w_j(x_k))).$$
(13)

## B. CTL Specifications Vs LTL Specifications

In specifying the property C3, we have seen that this property can be specified in CTL but cannot be specified in LTL. This could lead to a question: is CTL has more expressiveness power than LTL? the answer is no. To demonstrate this, we shall give a property to the system which can be expressed in LTL but cannot be expressed in CTL. For example: assume that we add a new property to the model such that

Every transaction started infinitely often is ended infinitely often

$$\bigwedge_{1 \le i \le n} \mathbf{GFr}_i(x_1) \Rightarrow \mathbf{GFend}_i.$$
(14)

This means that the transaction that becomes started infinitely often (and may become ended) must occur infinitely often. This kind of properties is called fairness property. Furthermore, if we need to ensure that every transaction is executed infinitely often such that:

$$\bigwedge_{1 \le i \le n} \mathbf{FG} \ end_i. \tag{15}$$

This property can be only specified in LTL.

#### V. CONCLUSION

In this research paper, We have given an LTL and CTL specifications for debit and credit transactions. These specifications can be used to verify a scheduler uses to schedule an unlimited number of debit and credit transactions that incoming and outgoing from a bank database system. we have assumed that the serializability is the correctness criterion for concurrent debit and credit transactions executing in a transactional processing system. We have shown that the transactional system and its properties can be specified and encoded using temporal logics. Also, in this paper, we have introduced a transition structure to model the transactional system and its properties in terms of propositions. This propositions represent the read and write operations from different transactions that become true (executed) at this state. The verification part can be executed by model checkers, such as NuSMV, to test whether the database scheduler satisfies the relaxed serializability condition and its properties or not. In case of no, counterexamples to show the errors are automatically given by the model checker.

We have found that temporal logics (LTL and CTL) are suitable to specify the relaxed serilaizablity condition. Actually, we encoded the (infinite or finite) histories of the debit and credit transactions in terms of read and write propositions in the transition structure that we defined. This means that we can prove that the histories, produced by the concurrent execution of debit and credit transactions in a scheduler, are serializable if

$$\sigma_{dct} \Rightarrow \sigma_{rcs}.$$
 (16)

is satisfied.  $\sigma_{dct}$  represents the temporal logic formula that specifies the behavior of the history in transition structure, that we have given above, and  $\sigma_{rcs}$  represents the temporal logic formula that specifies the relaxed serializability condition. This approach gives a fully automatic verification method that can overcome the disadvantages of the traditional approaches such as the user should understand in detail why the system works correctly (deductive verification), human error (mathematical proofs) and may not cover all possible system behaviors as in the simulation [21].

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