

A Comparative Performance Analysis of Low Power Bypassing Array Multipliers

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Abstract— Low power design of VLSI circuits has been identified as vital technology in battery powered portable electronic devices and signal processing applications such as Digital Signal Processors (DSP). Multiplier has an important role in the DSPs. Without degrading the performance of the processor, low power parallel multipliers are needed to be design. Bypassing is the widely used technique in the DSPs when the input operand of the multiplier is zero. A Row based Bypassing Multiplier with compressor at the final addition of the ripple carry adder (RCA) is designed to focus on low power and high speed. The proposed bypassing multiplier with compressor shows high performance and energy efficiency than Kuo multiplier with Carry Save Adder (CSA) at the final RCA.

Index Terms— Bypassing, Low Power, Speed, CSA, RCA, Compressor

I. Introduction

In modern VLSI system, power is the most important parameter to optimize for low power applications like Digital Signal Processor (DSP), portable devices etc. DSP is one of core technologies for multimedia and mobile applications, most DSP applications entail addition and multiplication arithmetic operations. Especially, the multiplier is the critical arithmetic operation unit for many DSP applications, such as filtering, convolution, Fast Fourier Transform (FFT), etc. Analysis of the conventional DSP applications shows that the average of zero input of operand in multiplier is 73.8 percent. An important low power design to reduce power consumption is to shutdown part of a circuit while it is not in operation. The power reduction in multipliers can be achieved using bypassing technique in DSP's. The primary power reductions are obtained by tuning off MOS components through multiplexers when the operand of the multipliers are zero^{[1][2]}.

The major source of power dissipation in CMOS circuits is the dynamic power dissipation. Dynamic power dissipation appears only when a CMOS gate switches from one stable state to another. In this paper we present a technique to minimize power dissipation in digital multipliers, from dynamic power of the total power consumption the concentration is on switching activity. There have been proposed a lot of techniques to reduce the switching activity of logic circuit^{[3][4][5][6][7][8]}. Bypassing is the extensively used technique for the reduction of major part of the total power consumption i.e dynamic power. Multiplication operation requires more computational time and higher circuit complexity. Many other complex arithmetic operations, like exponentiation, division, and multiplicative inversion, can be therefore performed by applying multiplication operations repeatedly. Hence, it is important in a practical sense to develop fast multiplication algorithms for these complex arithmetic operations. Not only to reduce power consumption, to enhance the speed of the bypassing multiplier (BM) also reported^[2]. Our contribution added a step ahead to improve the performance of the BM without increase of the power consumption.

The remaining organization of the paper is as follows: In Section 2 bypassing technique is discussed. Section 3 discusses the row based bypassing array multiplier. The proposed row bypassing multiplier with compressor is discussed in Section 4. The results and discussions are given in Section 5. Finally conclusion is given in Section 6.

1.1 Sources of Power Consumption in CMOS

Power consumption can be reduced in CMOS circuits by using a smaller design of multipliers like unsigned row and column bypassing multipliers. The sources of power consumption in CMOS circuits is given by

$$P_{total} = P_{dynamic} + P_{short\ circuit} + P_{leakage} \quad (1)$$
$$P_{total} = \alpha f_{clk} C_L V_{DD}^2 + I_{SC} V_{DD} + I_{leakage} V_{DD}$$

Dynamic power ($P_{dynamic}$) dissipation is the result of charging the load capacitances in a circuit, where α is the switching activity, f_{clk} is the clock frequency, C_L is the output capacitance and V_{DD} is the supply voltage. $P_{short-circuit}$ is the power dissipation due to direct path from V_{DD} to GND. There are six main sources of leakage current ($P_{leakage}$) in a CMOS transistor

1. Reverse-biased junction leakage current (I_{REV})
2. Subthreshold (weak inversion) leakage (I_{SUB})
3. Oxide tunneling current (I_{OX})
4. Gate direct-tunneling leakage (I_G)
5. Gate induced drain leakage (I_{GIDL})
6. Punchthrough current (I_{PT})

Currents I_2 , I_5 , and I_6 are off-state leakage mechanisms, while I_1 and I_3 occur in both ON and OFF states. I_4 occurs in the off state, but typically occurs during the transistor bias states in transition [9][10][11][12][13].

II. Bypassing Techniques

The key idea of this design is based on the observation that the most modern multipliers produce a large number of signal transitions while adding zero partial products. The design uses another way to transition activity optimization, and that is hardware bypassing. Since, adding zero partial products generate a large number of signal transitions in the carry-adder array without affecting the results and the additions bypasses by disabling the adders.

2.1 Row Bypassing

For a low power row bypassing multiplier, the addition in the j^{th} row can be disabled to reduce the power dissipation if the bit b_j in the multiplier is 0, i.e., all partial products $a_i b_j$, $0 \leq i \leq n-1$, are zero. As a result, the addition operations in the j^{th} row of CSA is in the Fig. 1 is bypassed and the outputs from the $(j-1)^{th}$ row of CSAs is directly fed to the $(j+1)^{th}$ row of CSAs without affecting the multiplication result. In the design, each modified FA in the CSA array is attached by three tri-state buffers as shown in Fig. 2. The tri-state buffer shown in Fig. 3 decides whether to disable the full adders or not according to the multiplier bits b_j . And then utilizes two multiplexers as shown in Fig. 4 to select the correct outputs. The extra correcting circuits must be added to correct the multiplication result.

When the corresponding partial product is zero, the RBAC disables unnecessary transitions and bypasses the inputs to outputs. Two multiplexers augmented to the outputs of the adder transmit the input-carry bit and the input-sum bit of the previous addition to the outputs.

The tri state buffers placed at the input of the adder cells disable signal transitions in the adders which are bypassed, and the input carry bit and input sum bit are passed to downwards.

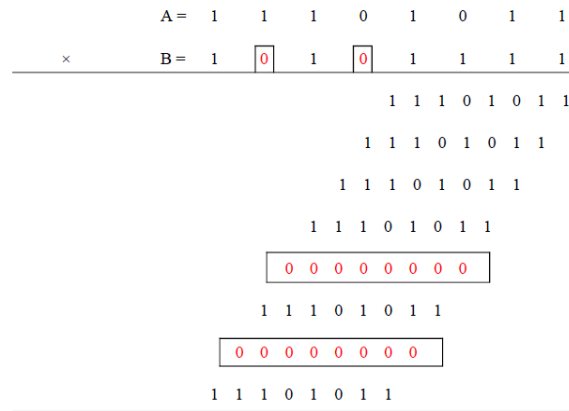


Fig. 1: A 8×8 multiplication of bit $b_j = 0$ corresponds to column $j = 0$

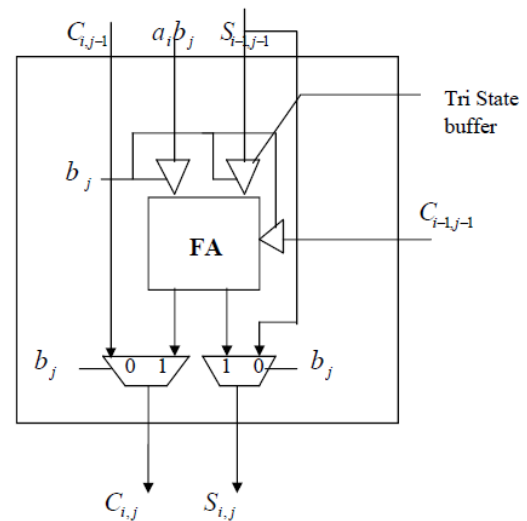


Fig. 2: Row Bypassing Adder Cell

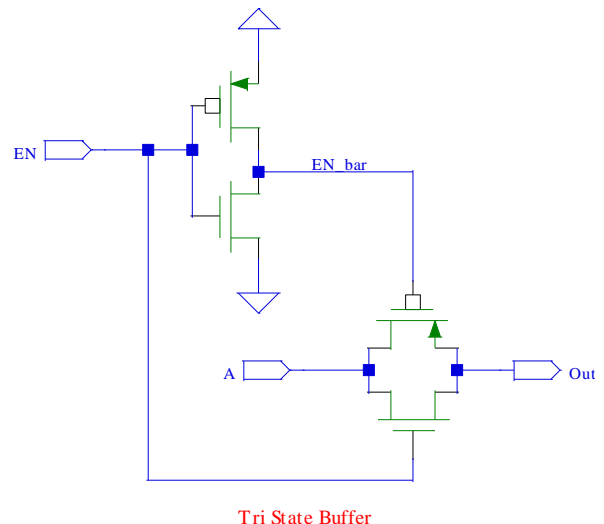


Fig. 3: TGCMOS Tristate Buffer

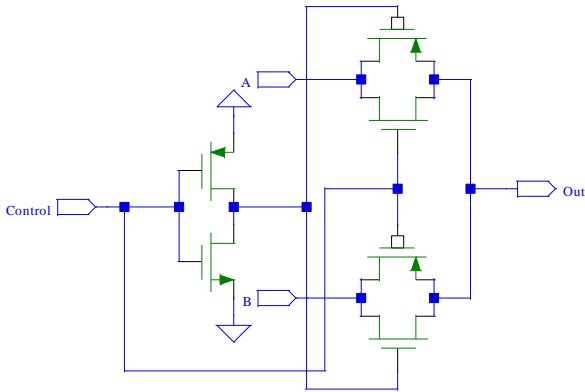


Fig. 4: TGCMOS based 2-1 Mux

2.2 Column Bypassing

Instead of bypassing rows of Full adders, columns of Full adders of the multiplier design are bypassed. In this approach, the operations in a column can be disabled if the corresponding bit in the multiplicand is 0. There are two pro of this method. First, it eliminates the extra correcting circuit. Secondly, the modified FA is shown in Fig. 6 is simpler than that of used in the row bypassing multiplier.

Theorem: When $a_j = 0$, the output of a column j adder cell $FA_{i,j}$ can be specified as follows:

1. The output carry bit is 0.
2. The output sum bit is equal to the output sum bit of $FA_{i-1,j+1}$.

Proof: 1. Consider row 0. Note that, in row 0, there are only two bits to be added. Adder $FA_{0,j}$ carries out $a_j b_1 + a_{j+1} b_0$. If $a_j = 0$, then the output carry bit must be zero, and the out sum bit is equal to $a_{j+1} b_0$.

2. Assume that the theorem holds for row i .
3. In row $i+1$, the inputs of $FA_{i+1,j}$ are carry bit from $FA_{i,j}$, sum bit from $FA_{i,j+1}$, and the partial product $a_j b_{i+1}$. Since $a_j = 0$, two out of the three inputs are 0, and the output sum bit is equal to the sum bit sent by $FA_{i,j+1}$. The column bypassing if $a_i = 0$ is as shown in Fig. 5.

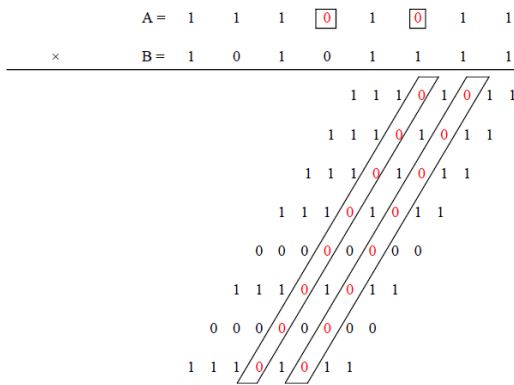


Fig. 5: A 8×8 multiplication of bit $a_i = 0$ corresponds to column $i = 0$

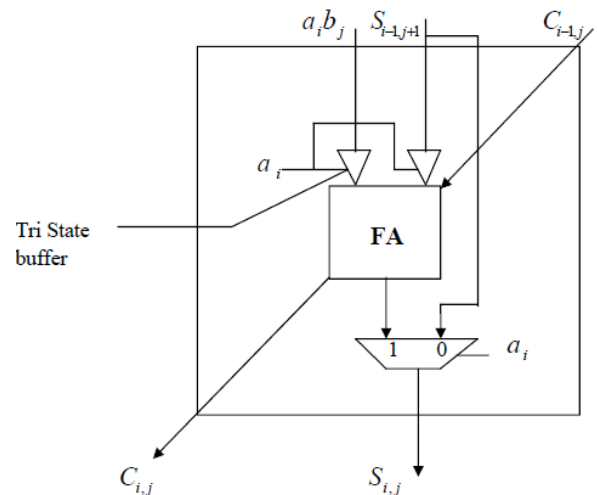


Fig. 6: Column Bypassing Adder Cell

The two tri-state buffers are placed at two inputs of full adder to disable the operation of full adder when a_j is 0. The tri-state buffer is designed by TG-CMOS. The multiplexer is placed at the sum output of full adder. The value of sum is selected from the bypassing value or sum output of full adder according to the value of a_j . This bypassing cell does not need to add multiplexer for carry output and tri-state buffer for carry input of full adder. Therefore, significant portion of extra hardware is saved without degrading the performance. In addition, power consumption can be also reduced as an effect of reduced hardware activities.

III. Bypassing Array Multiplier

In numerous computing and signal processing applications, parallel multiplier has been a building block for many algorithms. The Carry-Save Array (CSA) multiplier is a straight forward implementation of vector multiplication. It consists of a partial product reduction tree, which is used to calculate partial products in Carry-Save redundant form, and a final chain adder to transform the redundant form in normal binary form. The functionality of the Carry-Save array multiplier is as follows. $X = (x_{n-1} \dots x_0)$ and $Y = (y_{n-1} \dots y_0)$ are fed into an array of FA cells. Each FA cell performs the multiplication $X_i \times Y_i$ using an AND gate and then adds the result with the incoming carry bits, to produce an output sum and an output carry. All FA cells are appropriately connected (sums and carries) to perform the multiplication. The final adder is used to merge the sums and carries from the last row of the array, since in every row the carry bits are not immediately added but rather propagated to the row below. The column bypassing multiplier using CSA is as shown in Fig. 8 with Column Bypassing Adder Cell shown in Fig. 6.

IV. Row based Bypassing Multiplier with CSA

The Bypassing scheme is used for low power applications of the processor. The method is used to disable the gate if the input operand of the multiplier is zero. To focus on the speed of the multiplier a design was proposed shown in Fig. 9, in which CSA architecture is used at the final addition [2]. For an example, 8x8 multiplication can be divided into two 8x4 bypassing multiplier based on RCA as shown in Fig. 7.

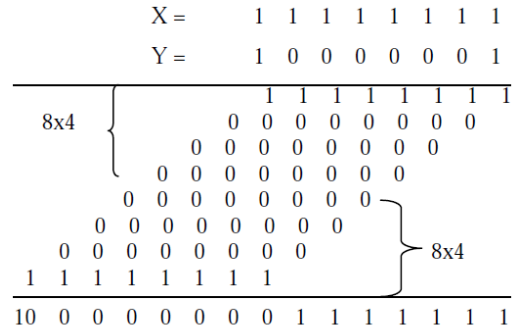


Fig. 7: 8x4 Partial product reduction into two parts

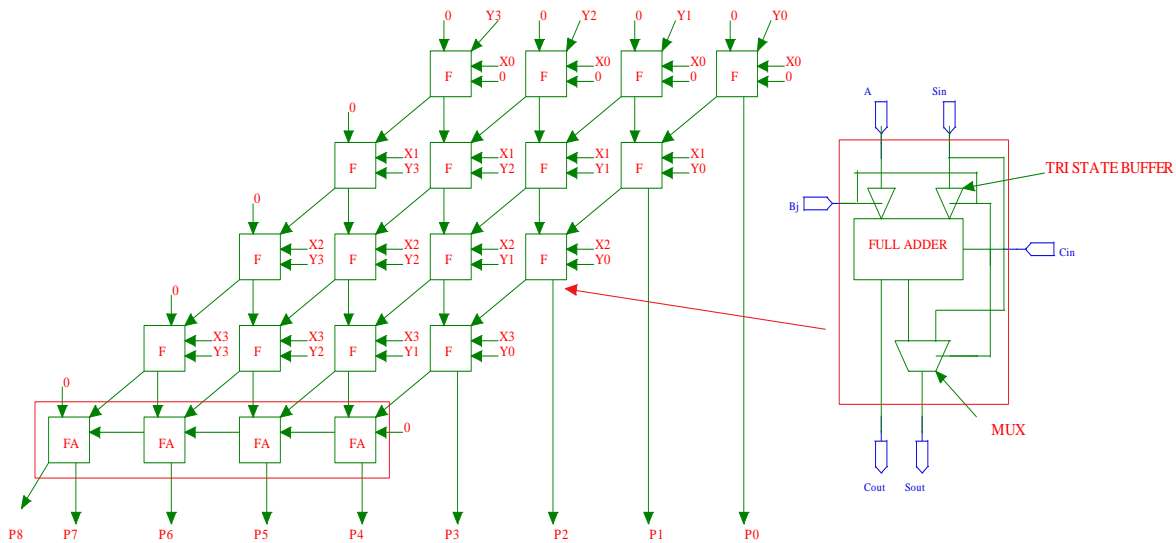


Fig. 8: Schematic design of Column Bypassing Array Multiplier

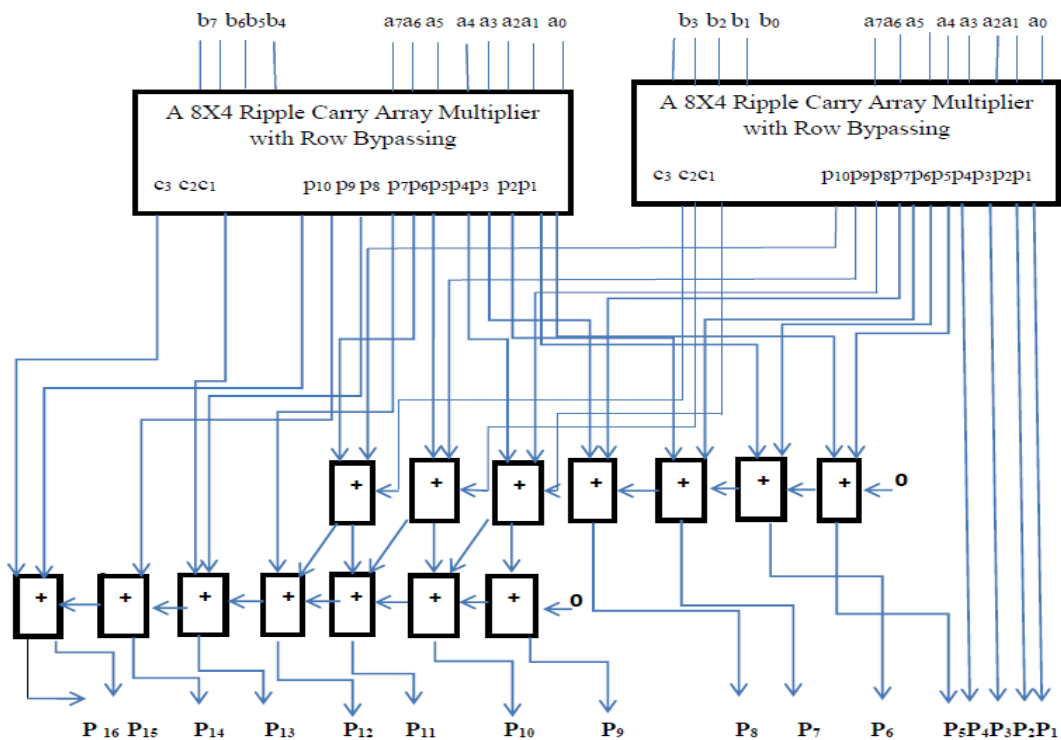


Fig. 9: Row based Bypassing multiplier with CSA at final addition [2]

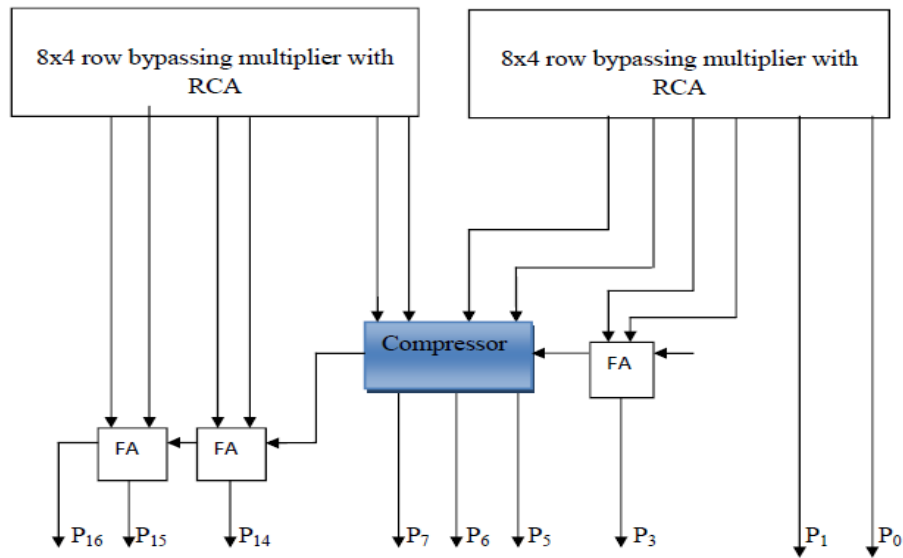


Fig. 10: Row based Bypassing Array Multiplier with Compressor at final addition

The partial sums and carry output from these two 8x4 multipliers can be computed simultaneously. Note that the final stage adders consist of RCA adders in both sides and CSA adders in the middle. In this configuration, the parallelism of the existed multiplier can be established. Furthermore, delay time of RCA multiplier can be shortened through this method.

4.1 Proposed Row based Bypassing Multiplier with Compressor

In this paper, the proposed multiplier shown in Fig. 10 adopts parallel architecture to shorten delay time further than that of the multiplier shown in Fig. 9. This proposed multiplier consists of a compressor at the middle of RCA further to accelerate the speed of the multiplier. For example, in an 8x8 multiplication the 8x4 two partial product blocks with bypassing method based on RCA with compressor design is shown in Fig. 10. The partial sums and carry output from these two 8x4 multipliers can be computed simultaneously. Note that the final stage adders consist of RCA adders on both sides and compressors at the middle. With this configuration, a parallelism of the proposed multiplier can be established and also the delay can be reduced with somehow having extra hardware.

Minimizing the number of resources required within a processor would have a positive impact on its power performance. Furthermore, since an adder is one of the basic arithmetic units, any improvement in the performance of an adder would have a major impact on the performance of a processor. Multi-operand adder structures are frequently used for the summation of partial products in multiplication, as in the Wallace and Dadda tree multipliers. They are also used in the implementation of arithmetic expressions arising from the conversion of constant multiplications into shifts and additions [14][15][16].

The 14-T full adder design used to design the compressor is as shown in the Fig. 11. The performances of the full adder with other full adders [17] [18] are as shown in the Fig. 12.

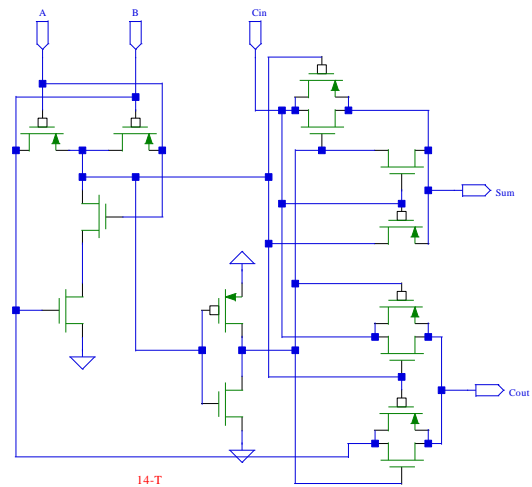


Fig. 11: Schematic diagram of 14-T full adder

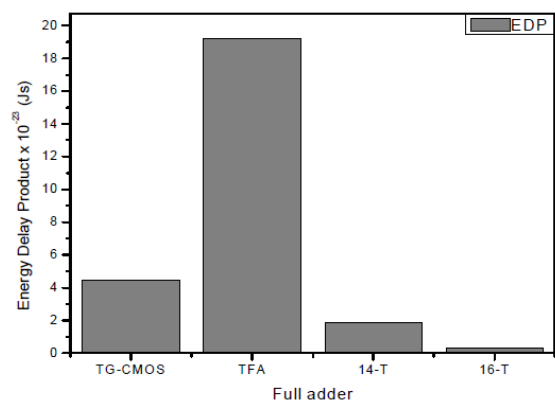


Fig. 12: EDP of the different full adders for 180nm technology

Compressors do the simple operation of addition that adds more number of bits at a time.

Different compressors logic based upon the perception of the counter of full adder, a single bit full adder can be considered as a counter of “1,s” at the input bits. It can be defined as single bit adder circuit that has four/five/six/seven inputs and three outputs.

The Wallace tree architecture supports fully parallel partial product reduction. The classic 3-input Wallace tree element is a carry-save adder which accepts 3-bit wide operands and exports a 2-bit wide result, i.e., the 3-2 compressor takes 3-inputs of same weight and produces 2 outputs, a sum of weight 1 and a carry of weight. 2. Given the nature of the 3-2 compressor, it is impossible to build completely regular tree architecture.

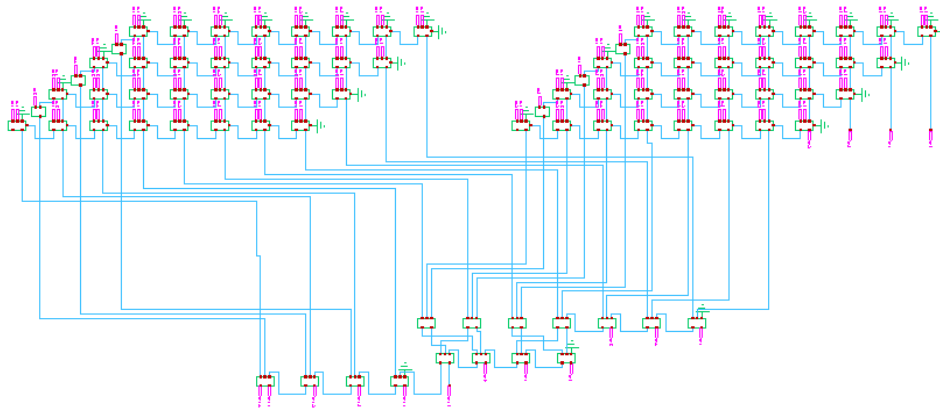


Fig. 13: RBM Comp design impementation

V. Simulation Results and Discussions

The design implementation using Tanner EDA tool is as shown in Fig. 13. The performance evaluation of the all the bypassing multipliers are done by Synopsys

HSPICE for 180nm technology with a supply voltage of 1.8V. Table 1 shows the performances of the bypassing multipliers in terms of power, delay, energy delay product (EDP) and number of MOS components.

Table 1: Performance Comparison of the multipliers

Multiplier	Power (mW)	Delay (ns)	EDP (js)	Transistors
CBM	11.91	0.95	1.07E-20	1904
RBM	14.24	1.45	2.99E-20	2336
RBMCSA [2]	13.30	79.56	8.42E-17	2408
RBM Comp	13.36	1.45	2.81E-20	2422

The proposed RBM using compressors can consume little more power 13.36 mW than [2] 13.3 mW because of the one extra full adder as shown in the Fig. 14. Due to extra hardware the RBM consumes more power than CBM.

RBM Compressor design shows high speed 1.45 ns than that of the RBMCSA 79.56 ns as shown the performances in the Fig. 15. The vertical compression of the compressors due to parallel nature enhances the performance of the RBM Comp. MOS components of the implemented designs are also given in the Table. 1. Though the proposed requires one full adder, the proposed multiplier is energy efficient than RBM and RBMCSA. All multipliers are implemented with 14-T full adders. Therefore the proposed requires 14 additional transistors.

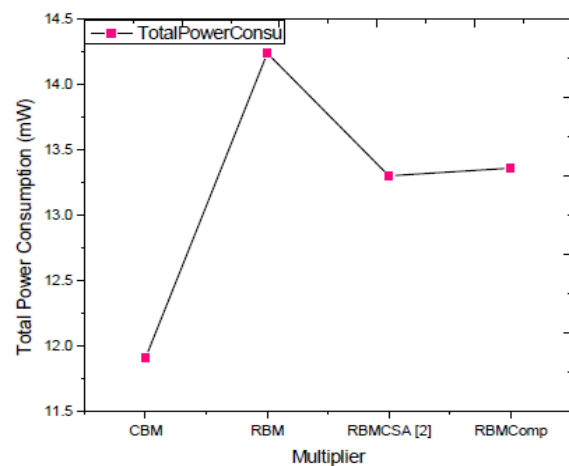


Fig. 14: Total power consumption of the multipliers

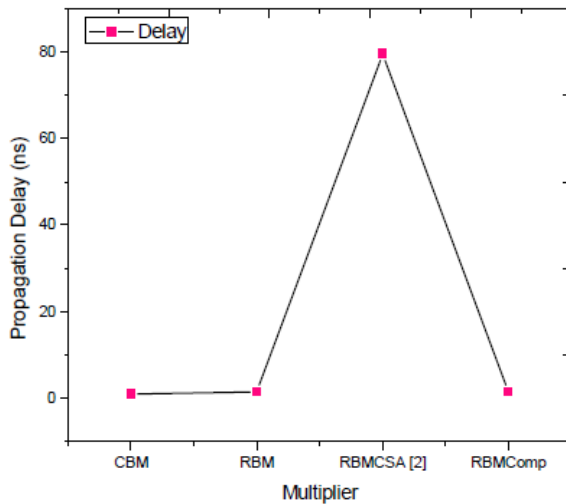


Fig. 15: Performances of the multipliers

VI. Conclusion

Low power designs are mandatory nowadays for DSPs and battery powered portable electronic appliances. The arithmetic operations of DSPs must be performed for low power consumption without loss of the performance. The prominence of this paper is without increase of the power consumption to accelerate the performance of the multiplier using bypassing technique. Column bypassing cell is used in row bypassing technique for fewer transistors in order to decrease the power consumption. In this paper a step is taken further on to increase the speed of the multiplier further using a compressor is designed with full adders and placed at the middle of the final addition of the RCA. The RBM Comp multiplier consumes little more power with the enhancement of speed and also saves more energy by consuming one full adder area.

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