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Performance Evaluation of the Loop Buffer Switch under Prioritized Traffic

Mr. **Devesh Pratap Singh**
B.B.D. University, Lucknow, India
E-mail: deveshpratap.85@gmail.com

Dr. **Rajiv Srivastava**
Indian Institute of Technology, Kanpur, India
E-mail: rajivs@iitk.ac.in

***Abstract*—** In this paper, optical loop buffer based architecture is discussed; with its advantages over other architectures. In general the performance of the switch is measured at physical and network layer. The physical layer analysis deals with power budget analysis, however, at the network layer; the performance is measured in terms of packet loss probability and average delay. To obtain more realistic performance at the network layer the QoS parameters need to be included. In this paper, a QoS parameter which is known as priority of the incoming packets is included and corresponding results are presented, and it has been found that even at the load of 0.7, packet loss probabilities on the order of 10^{-5} can be achieved.

***Index Terms*—** Optical Loop Buffer, Priority, TWC (Tunable Wavelength Converter)

I. Introduction

The Internet has already reached an enormous complexity, and it is still rapidly growing. A wide variety of new services has emerged. Real time and multimedia applications such as internet telephony, video-conferencing, video on-demand and many others make high demands on future networking solution such as increasing capacity and appropriate quality of service (QoS) provisioning. In particular, higher quality of service is required. Hence, providing faster transmission technologies and supporting differentiated QoS are major challenges for the future-generation internet. Optical networks are promising to meet these demands. Multiple wavelengths within a single fiber can be handled by wavelength division multiplexing (WDM). Photonic packet switching architectures are capable of support high-speed operation by occupying wavelengths only for the time needed to transmit packets. In optical networks, packet loss is a common phenomenon. As the network, or its links or any node (i.e. photonic packet switches), becomes congested, the switch buffer becomes full and starts to drop packets. For non-real time applications, such as file transfer, e-mail, packet loss is not critical. But in real-time applications (i.e. voice, video), packet loss means unintelligible information. Also in real time applications, packet should reach their destination with the least amount of delay. Although transmission in optical packet networks is very fast and in general packets, delay could be lower than electronic packet networks, some applications (services) demand better packet delivery guarantees. The solution of QoS is service differentiation (prioritization of data or packet) in packet networks with big traffic load.

The optical network composed of core and client network, in the core network optical packet switches are placed as to support higher data rate. As in the core network optical switches are main elements, hence many optical packet switch architectures are proposed and demonstrated [1] [2] [3] [4] [5]. In this paper, a loop buffer based is considered and performance of the architecture is measured in terms packet loss probability under prioritized and non-prioritized traffic.

The paper is organized as follows. In the Sect. 2, overview the related work and architecture description is detailed. In Sect. 3, Performance measure of the loop buffer based architecture is discussed. In the sec. 4, simulation results are presented, and finally, Sect. 5 discusses the major conclusions of the paper.

II. Related Work and Architecture Description

The overlay structure of the network is shown in Figure 1. The network is composed of edge and core routers. The Edge routers act as an interface between clients and core network. The core routers are optical, while edge routers are electronic in nature. The control operation of the core and edge routers is performed by the electronics. The edge routers placed at the boundary of the network are capable of packet aggregation. The ingress edge router receives packets from the client network and converts it in appropriate format and directs the aggregated packet towards core routers. The

electronic edge router is assumed to include electronic RAM's, optical TDM and switch fabric for buffering, aggregation and forwarding of packets. The backbone networks, where large numbers of aggregated data packets flows at a very high data rate will be optical in nature.

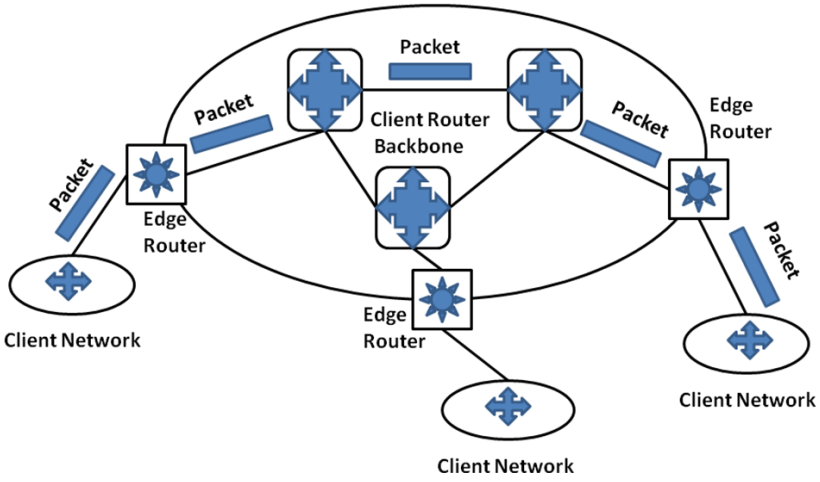

Fig. 1: Overlay structure of the network

Photonic packet switches utilize both large capacity of the optical fiber for data transmission and mature electronics for the control operation. Thus the growing internet traffic demands can be catered to using photonic networks. At the switching nodes as shown in Figure 1 in the optical packet switched networks, data pass through in optical domain [3]. The control logic for these switching nodes is usually implemented in electronic domain. In photonic switching, data is transported in short blocks (called packets or cells) as in most of the currently existing electronic network like ATM (Asynchronous Transfer Mode), TCP/IP (Transmission Control Protocol/Internet Protocol) etc.. The packet contains two segments: header and payload. The header is encoded at lower bit rate, and contains information such as source address, destination address etc.. The payload contains actual data and encoded at the data rate ranges from a few Mbps to some tens of Gbps. The important components of a photonic packet switch [3] are control, packet routing, packet synchronization, clock recovery, contention resolution, buffering and packet header replacement. In the optical packet switching, buffering will be required when two or more packets arrive for the same output port in same time slot. Then, one of the contending packets will be directed to the output port, and rest of them, have to be stored in random access memory (RAM). Till now, all optical RAMs for photonic packet switching has not yet been developed. For the contention resolution, three solutions can be used:

1) Fiber delay lines (FDL) in traveling and recirculating configuration in time domain.

2) Deflection routing in space domain.

3) Wavelength conversion of the data in wavelength domain.

In this paper, FDL based switch architecture is considered. At the input of the switch, packets can arrive synchronously or asynchronously and the arriving packet may be of same or variable lengths. It has been found in previous study that switches, at which packets of equal lengths arrive synchronously, have better performance. Furthermore, recently [6] has shown that optical components don't have much advantage over electrical components in term of power consumption some time; they consume even more power [6]. Thus, it is believed that hybrid scheme; in which core network is optical in nature while edge routers will be electronic in fashion, is the better choice [7].

Many optical packet switch architectures for the core network have been reported in [1] [2]. All of them have their advantages and disadvantages, and their comparative study is performed in [8].

The first loop buffer based architecture (Figure 2) was proposed by bendelli [2]. This architecture requires a very large number of components for buffering; semiconductor optical amplifier (SOA), and also the size of the demux and mux effectively scales linearly with required number of buffer wavelengths. Thus physical loss of the architecture is very large. The main limitations of the SOA based architecture are:

1) Simultaneous read/write operation is not possible, as SOA used as 'gate switch' and it has to be turned 'ON' and 'OFF' and both of these operations cannot be performed in single time slot.

2) Dynamic re-allocation of wavelengths is not possible.

3) Dynamic range of SOA is limited.

4) Crosstalk due to SOA is very high.

The above mentioned limitations can be mitigated using tunable wavelength converter (TWC), in place of SOA in the buffer [5] [9]. However, the TWC also has following limitations:

1) With the current technology the tuning range of the TWC is very limited.

2) Commercialized TWC are noisy device, and hence signal quality degrades when wavelength is tuned.

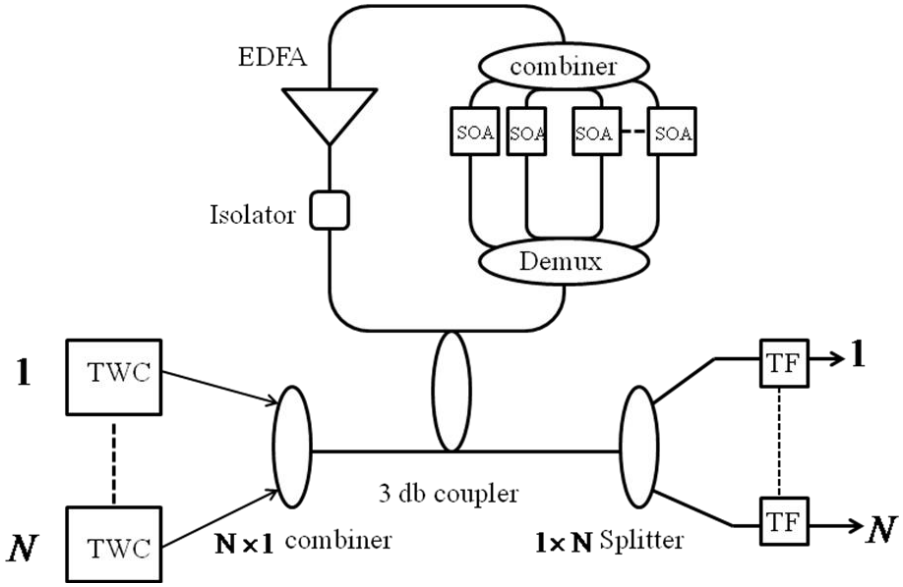

Fig. 2: Schematic of the considered architecture A1

In the Bendelli [2] architecture, later on modifications are suggested in the architecture to improve its performance. In the similar context, recently Choa proposed an architecture [1] which has lesser physical loss as compared to architecture A1. However, in terms of packet loss probability architecture A1 performs better than Choa's architecture [8]. In both of these architectures, packets in the buffer are controlled by the set of SOAs which acts as gate switches. The advantages of SOAs are fast tunability and compact size. Disadvantages are limited input power dynamic range and thus limited cascadability due to accumulated noise and gain saturation. In addition, the tunability of tunable filters (TFs) which is required at the output of the switches is another constraint parameter in these switches. These parameters limit the fundamental buffer depth (number of wavelengths used inside the buffer), and the accumulated ASE noise limits the number of packet re-circulations.

In the architecture, shown in Figure 1 further modifications are done, and resulted architecture is shown in figure 3.

The performance measure of the architecture is detailed in next section.

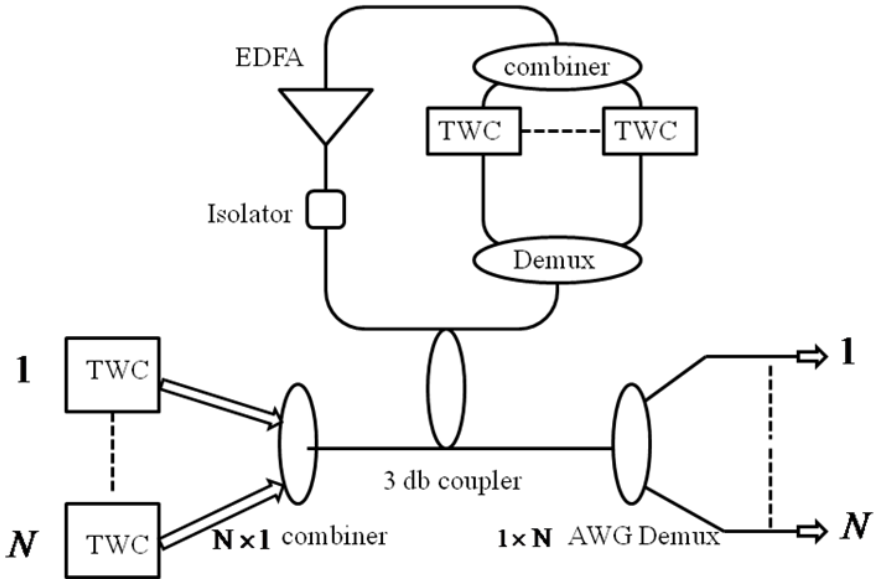

Fig. 3: Schematic of the considered architecture

In general, the optical switch with multi wavelength fiber loop as memory element has a very simplified structure and it uses single fiber delay line for the storage of the packets on different wavelengths. Packets from all the inputs use WDM technology to share the loop buffer [3]. The number of buffer wavelengths (size of memory) depends on the desired traffic throughput, packet loss probability, various component parameters and size of the switch [10].

III. Performance Measures of the Loop Buffer Based Architecture

Optical packet switches are the integral part of the optical core networks the architecture under consideration is shown Figure 3. This architecture is heavily investigated in the recent past due to its inherent advantages:

1) Simultaneous read/write capability
2) Dynamic re-allocation of wavelengths
3) Less control points

The description of the above-mentioned points in detail can be found in [8]. The design of any optical packet switch architecture is affected by nearly countless attributes. However, the most important one are described in Table 1.

Table 1: Critical Attribute and their Affect

Attribute	Effect	Reference
Attenuation	Scaling become Critical	[7]
Dispersion	Bit Rate gets limited	[8]
ASE Noise	Number of re-circulation gets reduced	[8]
FWM	Number of re-circulation gets reduced	[8]

The performance of the switch in terms of loss, power, noise and BER analysis is performed [11]. In the same paper, the detrimental effect of four-wave mixing (FWM) is also studied, and it is concluded that the architecture suffers from the re-circulation limits. Hence, to enhance the re-circulation count the placement of the regenerators inside the buffer is proposed in [12] [13] .The performance evaluation of the switch under random traffic is performed in [8]. However, in the generation of packets priority is not taken into account. Of the traffic, the priority is a QoS parameter and detailed in next section.

In this paper, the traffic priority is considered in the generation of packets, and correspondingly a modified algorithm is proposed, which will ensure good QoS. Finally, results are presented for prioritized and non prioritized traffic and compare has been made.

3.1 Quality of Service (Class of Service)

Services differentiation means categorizing traffic into different classes of priority, also called Quality of service (QoS) and applying QoS parameters to these classes or traffic with priority. To accomplish this, packets are first divided into different priorities by marking the type of service field in the packet header. Once the packets are classified at the edge of network, specific forwarding treatments are applied on each photonic switch. This combination of packet marking and well defined servicing procedure results in a scalable QoS solution for any given packet, and thus any application. Therefore, service's differentiation QoS approach is appropriate for the core optical packet networks where accurate QoS parameter (i.e. packet loss probability) for individual flows could not be assured because of difficulty in selective packet's control (storing, switching) in optical nodes but aggregated servicing could be well performed. In this work, the QoS attribute is packet loss probability. In a photonic packet switch, contention among packets occurs when two or more packets are to be routed towards the same output. In the case of wavelength conversion, the conflict is avoided unless all wavelengths on the loop buffer (fiber) are occupied. In real time applications, there are many services, which have higher QoS requirements; it means those services which cannot afford to lose any of its data or packet**.** In such a case, high-priority packets prior to low priority packets will be buffered, when both high and low priority packets need to be buffered. In case of inevitable packet loss (i.e. buffer wavelengths are not free); low priority packets are dropped before high-priority packets. Hence, the packet loss probability for high-priority service classes is significantly lower than for low priority classes. However, in any case, packet losses should be as small as possible, which means that packet losses are rare events, in particular for high-priority services.

3.2 The Traffic Model

In this paper, random traffic model is considered. This model is simple; still it provides good insight into the performance of the architecture, and also helps us to compare our result with previous publish results [9].This model assumes that the packet can arrive at any of the inputs with probability *P*, and each packet is equally likely to be destined to any of the *N* outputs with probability *1/N*. Thus, the probability that *Z* packets arrive for a particular output in any time slot is given by [14].

$$P_r(z) = \frac{N!}{(N-z)!z!}\left(\frac{P}{N}\right)^z\left(1-\frac{P}{N}\right)^{N-z} \quad (1)$$

In case of traffic with different class or priority, if $Q_1, Q_2, ..., Q_s$ denote the ratio *class-1, class-2, class-S* packets to the total number of packets; where *S* is the

number of priority classes (*1* is the highest, *S* is the lowest). Probability that n_1 *class-1*, n_2 *class-2*... n_s *class-S* packets arrive at the switch in a same time slot, is given by:

$$b_{n_1,n_2,\ldots,n_s} = P_r \sum_z (Q_1)^{n1}(Q_2)^{n2}.....(Q)^{ns} \frac{\sum_z (n_z)!}{\prod_z (n_z!)} \quad (2)$$

Where $Q_1, Q_2, ..., Q_s$ mean the ratio of *class-1*, *class2… class-S* packets to the total number of packets.

IV. Results and Discussions

For the switch architecture, the algorithm according to which the packets are forwarded to the output or stored into the buffer is as follows:

The switch uses (*B*+*N*) wavelengths, where *B* is the number of buffer wavelengths, and *N* is the number of wavelengths used for direct transmission to the output bypassing the fiber loop. The steps to be followed are:

1. All-optical wavelength converters at the inputs of the switch can be tuned to any of the (*B*+*N*) wavelengths instantaneously.
2. The buffer is such that read and write operations happen simultaneously in the same slot for the loop buffer wavelength.

4.1 Algorithm and design Considerations

If there are i $(1 \le i \le B)$ packets in the buffer for the output *j*, only one of *i* packets will be sent to the output *j*. if in the same slot, there are one or more packets also present at the inputs for the output *j*, then these will be buffered in the loop buffer to the extent allowed by rules 3 and 4. If all the buffer wavelengths are occupied, then remaining packet will be dropped.

Considering the case when there is *n* for the output *j*, but *m* input lines have packets in the buffer for that output, and then one of these *m* packets is directly sent to the output *j* in the switch. The remaining *m-1* packets will be stored in the buffer to the extent permitted by rules 3 and 4.

3. The number of packets X_j in the buffer for the output j should never be greater than B, i.e. $X_j \le B$ for j = 1 to N.
4. The total number of buffer space used should never exceed B, i.e.
$$\sum X_j \le B.$$

Throughout the paper in the simulation, the size of switch is assumed to be 4×4. In Figure 4 packet loss probability vs. load is plotted with buffering capacity of 4, 8, and 16, with load varying from 0.2 to 1 and traffic is without any priority. It can be clearly observed from the figure that for the 4×4 switch, *B* = 8 is the acceptable switch configuration. For *B* = 8 the packet loss probability for the lower loads (less than 0.5) is below 10^{-6}. At the load of 0.6 for *B* = 8, the packet loss probability is below 10^{-4}, whereas for *B* = 4 it is closer to 10^{-2}. Hence, *B* = 4 can be considered as very small buffer space. For *B* = 16, the packet loss probability is 10^{-4} even at the load of 0.8. It means as load increases, to maintain the same packet loss probability, more buffer space is required.

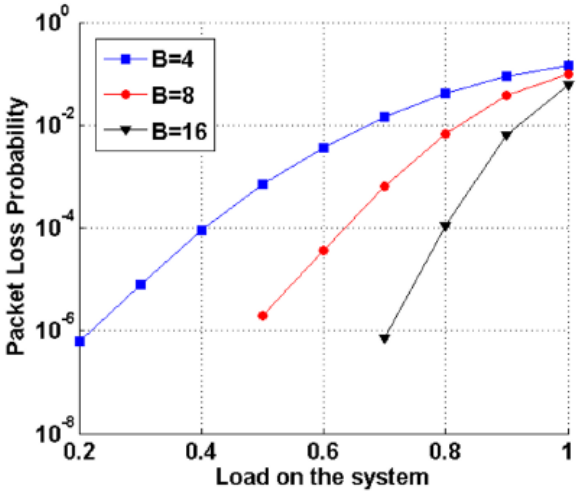

Fig. 4: Packet loss probabilities vs. load for different buffer space (Traffic without priority)

4.2 Traffic with Priority (Without Re- circulation Limits)

1. In any slot, if there are one or more packets present in the buffer or in the input lines for output *j*, then the packet would be sent to the output *j* following the rules 2 and 3. After repeating rule 2 and 3 for each output, remaining packets in the input lines would be buffered following rule 5-6. Any leftover packets will be dropped.
2. If there are only two classes (priority) of packets namely high and low and there are packets in the buffer for the output *j*. If high-priority packets are in the buffer for output *j*, send one of them to the output *j*. If no high-priority packet is present in the buffer for output *j*, then in that slot check all inputs of the switch for a high-priority packet for the output *j* and if one or more high-priority packets are present in the input for output *j*, send one of them to the output *j*. if no high-priority packet is sent to output *j*, go to rule 5.

3. If there is no high priority packet for output *j*, neither in the buffer nor in input lines, then if there are low priority packets present in the buffer for output *j*, send one of them to the output *j*. And if there is no (neither high nor low) packet in the buffer for the output *j* and no high-priority packet in input lines for output *j* in that slot, then in that slot check inputs of the switch for a low-priority packet for the output *j* and if one or more low-priority packets are present in the input for output *j*, send one of them to the output j.
4. After applying rule 2-3 for each output, first check for high-priority packets in the input lines for any output and buffer them to the extent rule 5 and 6 allows. If all the high-priority packets in the input lines are buffered, then send the remaining low priority packets to the buffer following rule 2 and 3.
5. The number of packets X_j in the buffer for the output *j* should never be greater than B, i.e. $X_j \le B$ for j = 1 to N.
6. The total number of buffer space used should never exceed *B*, i.e.
$$\sum X_j \le B.$$

Let us defined factor *Q* (Quality factor), which is a measure of priority of packets:

$$Q = \frac{HPP}{HPP + LPP} = \frac{HPP}{TP} \qquad (3)$$

Where,

HPP=High Priority Packets

LPP=Low Priority Packets

TP=Total Packets

In the first simulation as shown in Figure 5 there are 50% high priority traffic and 50% low priority traffic of the total traffic. The buffer size is B = 8. It can be observed from Figure 5 that switch efficiently stores the high priority traffic. High priority packet loss probability at load 0.6 is below 10^{-6},which is almost negligible. At traffic load of 0.7, high priority packet loss probability is approximately 10^{-5} and low priority packet loss probability is nearly 10^{-3}. It can be inferred that the switch can provides better quality of service to high priority packets than low priority packets. The total packet loss probability matches exactly with the packet loss probability for traffic with no priority (Figure 4). So, the switch is giving good performance for high priority traffic without much deteriorating performance for the low priority traffic as they have low priority and loss of some of them can be afforded.

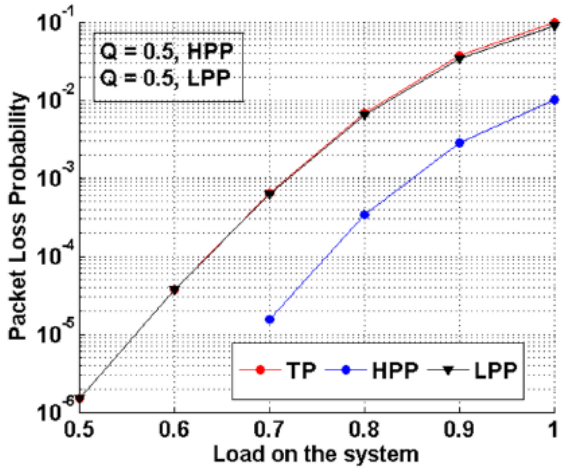

Fig. 5: Packet loss probability versus load on the system for high priority and low priority packets

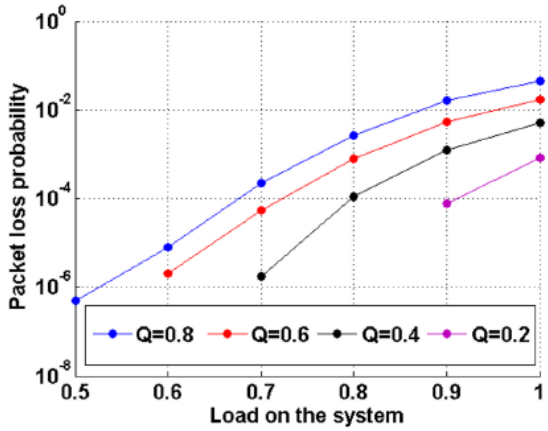

Fig. 6: Packet loss probability versus load on the system for varying high priority traffic load for N = 4, B = 8.

In Figure 6, comparison has been made between high-priority traffic, here Q = 0.2 signifies that in total traffic, 20% is high-priority traffic and 80% is low priority traffic. As we reduce the high-priority packets from the total traffic, the packet loss probability reduces. Up to the load of 0.7, the high-priority packet loss probability is around.

V. Conclusion

Quality of service is an important issue for the real time applications. Loss of information should be avoided as it will lead to unintelligible information. There is always a distinction between applications on the basis of priority. Some of them are highly prioritized. They must be provided better quality of service. Loop buffer based switch architecture provides better quality of service to the high-priority data. At the same time, it does not degrade the quality of service for the low-priority traffic.

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Authors' Profiles:

Mr. Devesh Pratap Singh

Mr. Devesh Pratap Singh received the B.Tech. degree in Electronic and Communication from U.P.Technical University, U.P, India. In 2009, he is currently pursuing his M.Tech. in Wireless Communication & Sensor Networking at B.B.D.University, Lucknow(U.P), India. He has been associated with Dr. Rajiv Srivastava from last three years as a photonic research group head. his research interests focus on the photonic packet switching, optical networks and wireless communication networks.

Dr. Rajiv Srivastava:

Dr. Rajiv Srivastava received the M.Sc. degree in physics (solid state) from CSJM University, Kanpur (UP), India, in 1997, and the M.Tech. degree in laser technology from the Indian Institute of Technology, Kanpur, in 2003. In 2009, he received Ph.D. degree from the department of Electrical Engineering Indian Institute of Technology, Kanpur. In 2009, he joined IITK as a senior project scientists. In the second half of 2009, he joined as visiting faculty in Indian Institute Technology Rajasthan. Currently, he is managing director of Ci-Edutech Pvt. Ltd. Kanpur. India. his research interests are in the fields of photonic packet switching, optical networks, mobile communications, and software development.

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