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FPGA Implementation of Digital Controller for Simple and Maximum Boost Control of Three Phase Z-Source Inverter

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Abstract— This paper presents, a high speed FPGA implementation of fully digital controller for three-phase Z-Source Inverter (ZSI) with two switching strategies include simple boost control and maximum boost control. In this method total of blocks are based on proposed digital circuits only with combinational logic and using pipelining technique. Since it is vital to have a high speed and effective ZSI controller, a novel digital design for pulse width modulation control have been implemented for simple and maximum boost control of the ZSI. The proposed digit controllers have been successfully synthesized and implemented by Quartus II 9.1V and Cyclone II FPGA, to target device EP2C20F484C6. Achieved result demonstrates that the proposed method has features including reconfigurable, low-cost, high speed and also it is very accurate.

Index Terms— ZSI, Simple and Maximum Boost Control, FPGA, Pipelining, Combinational Logic

I. Introduction

The function of an inverter is to change a DC input voltage to an AC output voltage of desired frequency and magnitude. Output voltage could be fixed or variable at a fixed or variable frequency. Variable output voltages are obtained by varying the input DC voltage with maintaining the inverter gain. Meanwhile, if the DC input voltage fixed and not controllable, variable output voltage can be obtained by adjusting the modulation index which is usually done by implementing Pulse Width Modulation (PWM) control within the inverter [1]. Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Hence, different circuit configuration namely Z-source inversion has become popular and considerable interest by the researcher is given to them [2]. The Z - source inverter has been proven experimentally and in the literature as an attractive single stage solution for buck-boost, three-phase DC-AC power conversion [3]. The Z-Source Inverter (ZSI) provides special features which can't be observed in the traditional Voltage Source Inverter (VSI):

- The Z-Source Inverter is a boost converter for DC-as power conversion and higher peak to peak AC output voltage can be obtained than available input voltage.
- A short circuit across any phase legs is allowed, so the dead time is not necessary. The cross conductive short circuit is called shoot through state and is similar to those in Current Source Inverter.
- Shorting of any phase legs provides a boost up capability thus must be carefully controlled.

As explained in above a short circuit across any phase legs is allowed, so control of transistors are very important. Two traditional control methods for ZSI are simple boost control and maximum boost control, we for creating a high accuracy and effective controller design a digital circuit. Features of this controller include reconfigurable, low-cost, high speed and also it is very accurate. The inverter controllers are included PWM, SPWM, modified SPWM, space vector PWM (SVPWM) and PWM proportional Z-Source Inverter (simple boost, maximum boost). These methods are implemented with two basic technologies according to control method. The first technology is based on devices include microcontrollers and DSP (Digital Signal Processor) with software control techniques, this group are implemented with high level language (C, C++, ...) and PWM signals and timers of microcontrollers and DSPs, thus this method is dependent devices and provides a rapid low-cost manufacturing solution for only special applications. However the for high-frequency switching power devices, with complex modulation schemes it is inappropriate. Some of researchers include [3] -[21] use these methods. For example for ZSI in [3] the authors present the optimal control of boost factor and capacitor voltage, reducing the voltage transistor stress under desired AC voltage level. Experiment implementation on TMS320F2812 DSP show possibility of accommodating blanking time DSP circuits for controlling shoot-through duty ratio without any additional external logic also a new configuration for ZSI was presented [21], with two inputs and outputs and is based on a nine-switch inverter. The control method is SVPWM that Prototypes of converters are

built using DSP. The FPGA comprises thousands of logic gates, some of which are grouped together as a configurable logic block (CLB) to simplify higher level circuit design. The simplicity and programmability of FPGA designate it as the most favorable choice for prototyping an ASIC. The advent of FPGA technology has enabled rapid prototyping of digital systems. However, with the advance of high-frequency switching power devices, complex modulation schemes can no longer be realized, even employing the most advanced digital signal processors, because of the high-speed switching requirement. This type of hardware architecture will become the major control scheme for advanced AC drives. Employing FPGA to realize PWM strategies provides advantages such as rapid prototyping, simple hardware and software design, higher switching frequency, and relieving the computation load of microprocessors. In recent years, motor control employing FPGA technology is receiving increased attention [22] –[30], for example in [24] used FPGA for implementation of the simplified SVPWM algorithm for three-phase voltage source inverter. In [25] used FPGA for multilevel multiphase Space Vector PWM algorithm. In [26] FPGA based multilevel pulse width modulation single phase inverter is implemented. In [27] an efficient strategy to generate high resolution three-phase pulse width modulation signal based on FPGA is implemented. In [28] implemented a simple realization of 5-segment discontinuous SVPWM based on FPGA and also on [29] an FPGA based digital space vector controller of voltage source inverter is implemented. But for ZSI only [30] presents a VHDL simulation of controller for ZSI suitable for Wind Energy Conversion System (WECS). The controller is designed and VHDL simulation carried out for traditional pulse width modulation as well as for the modified pulse width modulation employed with Z-Source Inverter. In [31] presents the design of a dual Z-source inverter that can be used with either a single DC source or two isolated DC sources. The dual inverter can be controlled using a carefully designed carrier-based PWM scheme that will always ensure balanced voltage boosting of the Z-Source Inverter while simultaneously achieving reduced common-mode switching. Because of the omission of dead-time delays in the dual-inverter PWM scheme, its switched common-mode voltage can be completely eliminated, unlike in traditional inverters, where narrow common-mode spikes are still generated. The presented PWM schemes can easily be modified to allow the inverter to operate without interruption. In [32], explores control methods for the current-fed Z-Source Inverter and their relationships of the current boost versus modulation index. A maximum boost control is presented to produce the maximum current boost under a given modulation index. The control method, relationships of current gain versus the modulation index and current stress versus current gain are analyzed.

This paper is organized as follows. In section II description of Z-Source Inverter is presented. Section III discusses developing a strategy for FPGA-based Z-Source Inverter controller and gives a detailed description of the digital circuit's scheme for controller. Section IV describes the comparison of the hardware implementation and chip utilization and also the simulation results taken from Quartus II that verify the performance of the proposed work. Section V is the conclusion.

II. Z-Source Inverter

As Explained in [33], the traditional inverters are VSI and current Source Inverter (CSI). The VSI based PWM VSI and CSI are characterized by relatively low efficiency because of switching losses and considerable EMI generation. Since switches are used in the main circuit, each is traditionally composed of power transistors and anti parallel diode. It provides bidirectional current flow and unidirectional voltage blocking capability. Thus inverter presents negligible switching losses and EMI generation at the line frequency. To avoid short circuiting of damaging deadline is allowing which provides a delay time between gating signals but it causes waveform distortion. In addition, both the V-source converter and the I-source converter have the following common problems.

- They are either a boost or a buck converter and cannot be a buck–boost converter. That is, their obtainable output voltage range is limited to either greater or smaller than the input voltage.
- Their main circuits cannot be interchangeable. In other words, neither the V-source converter main circuit can be used for the I-source converter, nor vice versa.
- They are vulnerable to Electromagnetic Interference (EMI) noise in terms of reliability.
- To produce any desired output a voltage, even greater than the line voltage, regardless of the input voltage, thus reducing motor ratings.
- Provide a ride-through during voltage sags without any additional circuits.
- Improve power factor reduces harmonic current and common-mode voltage.

In order to overcome the above problems of the traditional V-source and I-source converters, an impedance-source power converter. Fig. 1 shows the general ZSI structure. It employs a unique impedance network to couple the converter main circuit to the power source, load, or another converter, for providing unique features that cannot be observed in the traditional V- and I-source converters where a capacitor and inductor are used, respectively. The Z-Source Inverter overcomes the above-mentioned conceptual and theoretical barriers and limitations of the traditional

V-source converter and I-source converter and provides a novel power conversion concept. In Fig. 1, a two-port network that consists of a split-inductor L_1 and capacitors and connected in X shape is employed to provide an impedance source coupling the converter to load. The DC source can be a battery, diode rectifier, thyristor converter, fuel cell, an inductor, a capacitor, or a combination of those.

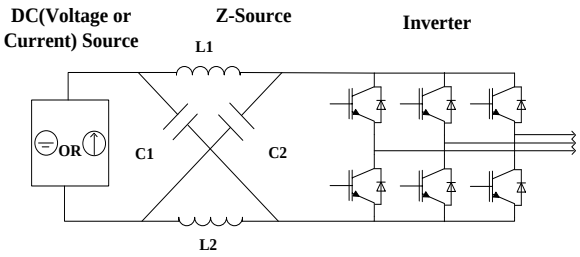

Fig. 1: General structure of the Z-source inverter

As seen in the Fig. 1 a three-phase ZSI configuration. The inductance L_1 and L_2 can be provided through a split inductor or two separate inductors. The three-phase ZSI bridge has nine permissible switching states (vectors) unlike the traditional three-phase V-source inverter that has eight. The traditional three-phase V-source inverter has six active vectors when the DC voltage is impressed across the load and two zero vectors when the load terminals are shorted through either the lower or upper three devices, respectively. This shoot-through zero state is forbidden in the traditional V-source inverter. This third zeroes start the shoot-through zero state, which can be generated by seven different ways: shoot-through via any one phase leg, combinations of any two phase legs, and all three-phase legs. The ZSI makes the shoot-through zero state possible. This shoot-through zero state provides the unique buck-boost feature to the inverter more detail for ZSI is presented in [33].

III. Switching Strategies and Implementation on FPGA

All the PWM schemes can be used to control the ZSI and their theoretical input–output relationships still hold. In every switching cycle, the two nonshoot-through zero states are used along with two adjacent active states to synthesize the desired voltage. When the DC voltage is highly desired AC voltage generates. But for ZSI and increase efficiency we use one modified carrier-based PWM control with shoot-through zero states that are evenly distributed among the three phase legs, while the equivalent active vectors are unchanged. Shoot-through zero state of ZSI can be in one leg, two legs or three legs. This paper implements two switching strategies include simple boost controls and maximum boost control that proportionally description in below:

3.1 Simple Boost Control Method

The best method for control and switching of ZSI is pulse width modulations. As described in [32], two PWM control methods, termed as the simple boost control method and the maximum boost control method has been explored, which result in the different relationships of the voltage boost inversion's ability versus the given modulation index M, because the aforementioned two methods can be regarded as the theoretical basis of various advanced PWM strategies such as the harmonic injection method and the space vector PWM method. It is seen from Fig. 2 that in the simple boost control, a straight line equal to or greater than the peak value of the three phase references is employed. The obtainable duty ratio of the shoot-through state can be regarded as a constant value, and its maximum value is limited to (1−M). As seen in Fig. 2 two straight lines V_p and V_n determined amount of surface pulse the shoot-through state. If the carrier (triangular waveform) greater of the V_p shoot-through zero is take place and also if carrier less of the V_n shoot-through zero is taken place.

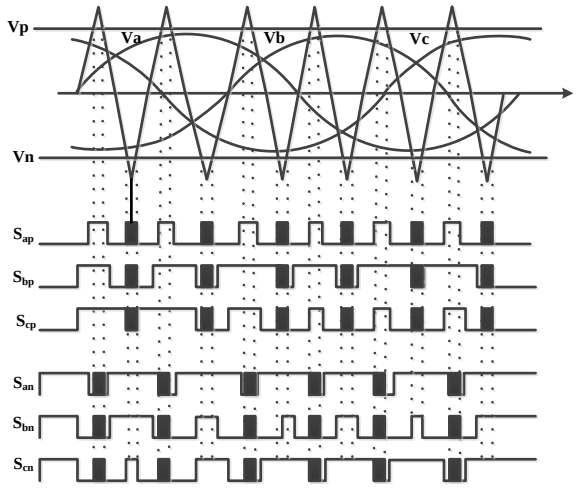

Fig. 2: Waveforms and switching strategies for the simple boost control

In following we present proposed digital design for this switching strategy and implementation it's on FPGA:

3.1.1 Proposed Implementation of Simple Boost Control on FPGA

The FPGA is standard integrated circuits that can be programmed by a user to perform a variety of complex logic functions. The FPGA has the capability of being reconfigurable within a system, which can be a big advantage in applications that need multiple trial versions within development, offering reasonably fast time-to-market. They also offer greater raw performance per specific operation because of the resulting dedicated logic circuit. Logic circuits are designed by the programmer in a software (two common languages for FPGA design are called VHDL

and Verilog), then transferred into the FPGA chip [34]. This proposed method is including three parts:

1. Generate sinusoidal signal

2. Generate a triangular waveform

3. Pulse generation module

3.1.1.1 Generate Sinusoidal Signal and Generation Strategy

In order to generate 50Hz sinusoidal signal we extract 360 points of each 220sin(x), 220sin(x+120) and 220sin(x-120) and put each of 360 points in proportional Look Up Table (LUT). So by each rising edge of the clock signal one of the samples of the sine wave is transferred to the output. LUTs are synchronous with the rising edge clock signal thus provided good continuity in production sinusoidal waveform and we have a continuous waveform actually. In other hand, in comparison stage triangular waveform and sinusoidal signals these operations are performed on all samples in each rising edge of the clock signal, so the comparison is synchronous with the clock and accuracy control method is very good. The input of LUT indeed is the same line addressing memory elements sinusoidal waveform samples stored in the LUT. Input lines of address are created by the address generator module. Proposed address generator module product address of x"000" to x"168" that equal 0 to 360 points of sine waveform. As shown in Fig. 3, the proposed address generator module first product address x"000" with each rising edge of the clock address generator is incremented one unit until address value equal with x"168" again state of address generator is change in x"000". Schematic of proposed address generator module is shown in Fig. 3. As seen in Fig. 3 with each rising edge of the clock adder is increase one unit, amount of output adder is addressed and transfer to the output register. One comparator is used for comparinge the last address (0x168) with output adder, if the last address detects output of D Flip-Flop is '0' so output register equal to zero, again address generator start with x"001" this cycle is repeated again.

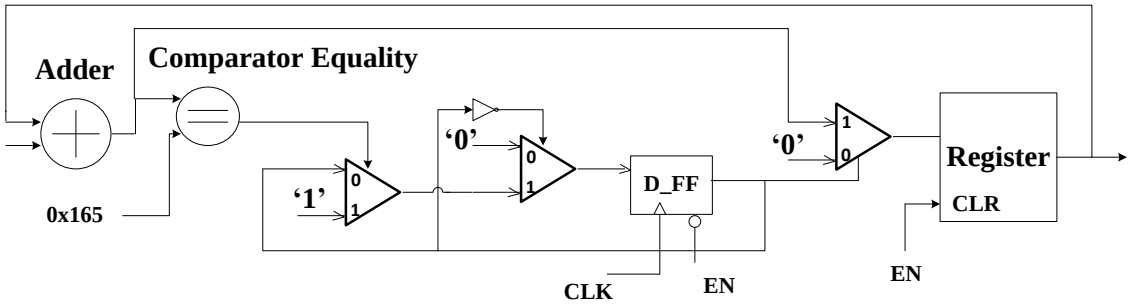

Fig. 3: Schematic of proposed address generator module

3.1.1.2 Generate Triangular Waveform

In order for the implementation of triangular waveform generator module use a counter with two modes, include negative number and positive number. One multiplexer is the use for switch between these modes. In this proposed circuit first mode is '0' counter start of "0" to a maximum number (for example 300) then the mode is '1' and counting to minimum number (for example -300) again mode be '0', thus triangular waveform is produced. Proposed digital design schematic is shown in Fig. 4 output D flip-flop is mode signal. In this circuit two comparators are used in proposed digital design one for comparing counter with maximum number and another for comparing counter with minimum number and also two adders are used in proposed digital design that one of adders is for increment one unit in mode '0' and another is for decrement one unit in mode '1'.

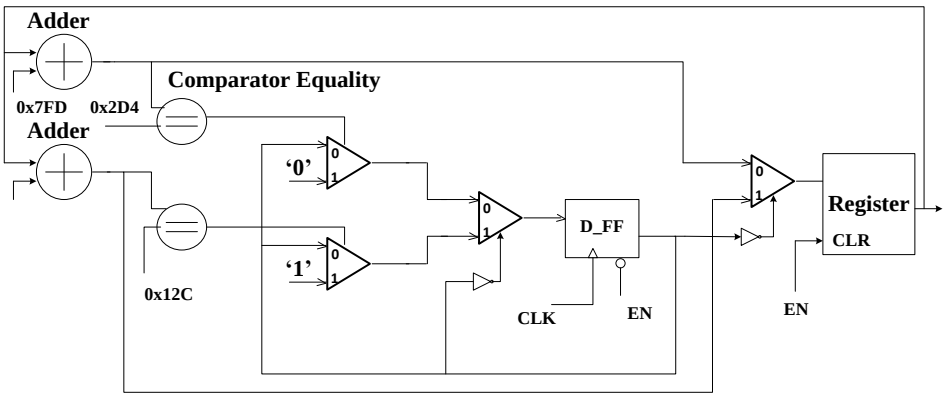

Fig. 4: Proposed digital schematic of triangular waveform generator

3.1.1.3 Pulse Generation Module

This block constitutes of three comparators so that with each rising edge of the clock one of the comparators compare one sample of the 50Hz sinusoidal waveform with one sample of 10KHz triangular waveform. If sample of 50Hz sinusoidal waveform is bigger than sample of 10KHz triangular waveform PWM_a output signal be '1' and PWM_na be '0' so that PWM_a is not PWM_na. Other comparators are for comparing V_n and VP with samples of a triangular waveform if the triangular waveform is greater than V_p shoot-through zero state is taking place also if triangular waveform be less than V_n shoot-through zero state is taking place. One of the advantage proposed circuit is totally of the sample triangular waveform is compared with Van and VP and each sample don't lose in comparison, thus comparison operation done completely because this circuit is synchronized with a clock signal. The PWM pulse is generated exactly. We increase speed by pipelining technique in proposed digital circuit. Pipelining is an implementation technique in which multiple data are overlapped in execution, also pipelining making digital designs fast. There are benefits in pipelining when the next data can process the following clock cycle. As a generic example in [35], consider the pipelined circuit. For each block, for example number i, are associated a maximum delay $t_{max}(i)$ and an average one $t_{av}(i)$. The latency and throughput of the circuit of Fig. 5 are equal to n. $T_{clk.}$

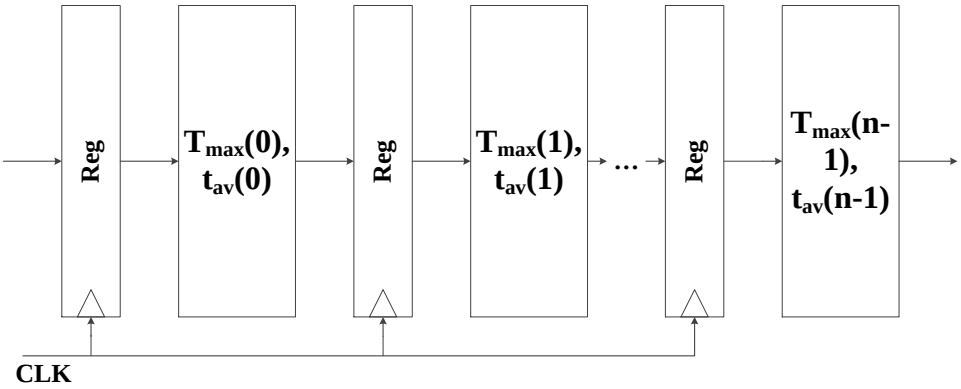

Fig. 5: Generic pipelined circuit

And $1/T_{clk}$, respectively where $T_{clk} > \max\{ t_{max}(0), t_{max}(1), \dots, t_{max}(n-1)\}$, that is,

Latency > $n.\max\{ t_{max}(0), t_{max}(1), \dots, t_{max}(n-1)\}$, Throughout < $i/\max\{ t_{max}(0), t_{max}(1), \dots, t_{max}(n-1)\}$.

In this design we apply pipelining technique by registers and two D Flip-Flops. Fig. 6 shows proposed digital design for only signals PWM_a, for PWM_b and PWM_c digital circuit is similar.

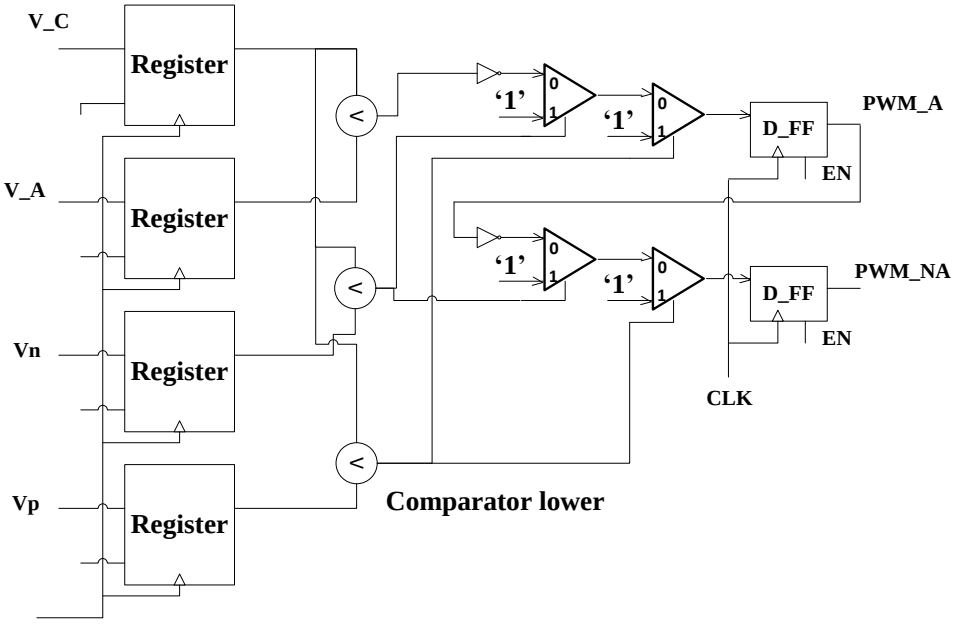

Fig. 6: Proposed digital design for signals PWM_a and PWM_na

As seen in Fig. 6, four inputs V_C, V_A, Vn and, V_P are getting with each rising edge of the clock. We use three comparators, one comparator for comparing samples of a triangular waveform (V_C) with samples of sinusoidal waveform (V_A), another for comparing triangular waveform (V_C) with the van and also a last comparator for comparing triangular waveform (V_C) with Vp. Multiplexers proportional output comparators determine '0' or '1' be signals PWM_a and PWM_na. Fig. 7 shows a total block diagram of proposed fully digital design simple boost switching on FPGA.

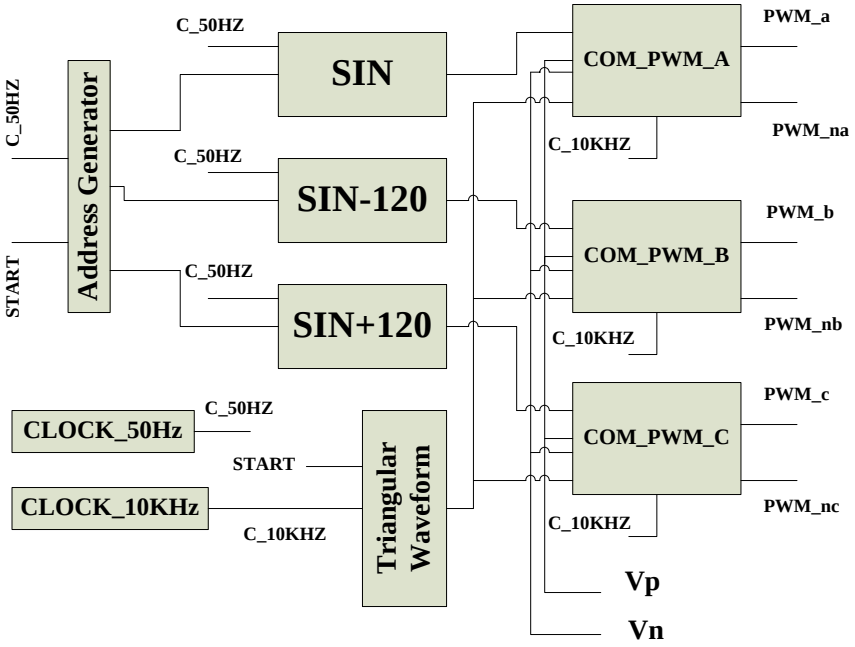

Fig. 7: Total block diagram of proposed fully digital design simple boost switching

3.2 Maximum Boost Control Method

For the maximum boost control method as shown in Fig. 8, the key point is that all zero states need to be turned into the shoot-through state so as to make the duty ratio as large as possible. Therefore, the shoot-through duty cycle varies in each cycle. As described in [32], reducing the current stress under a desired current gain now becomes important to the control of current fed ZSI. Therefore, to minimize the current stress for any given current gain, we have to minimize B (boost factor) and maximum M (modulation index), with the restriction that their product is the desired value.

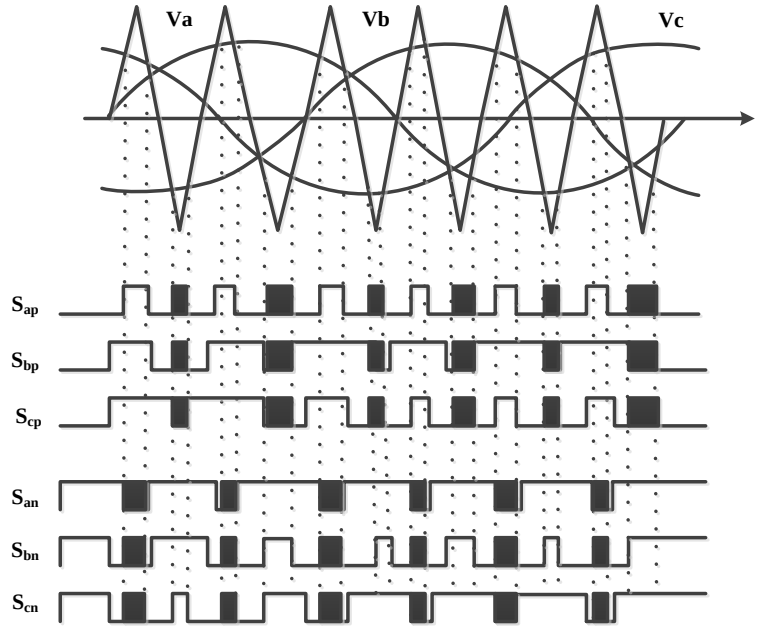

Fig. 8: Waveforms and switching strategies for maximum boost control

3.2.1 Proposed Digital Circuit for Implementation of Maximum boost Control on FPGA

The proposed implementation of maximum boost control on FPGA is similar to method for simple boost control, but the only pulse generation module is different. In the proposed digital circuit we use six comparators for comparing signals 220sin (x), 220sin (x+120) and 220sin (x-120), with triangular waveform. In maximum boost control for shoot-through zero state if the triangle waveform is greater than three sinusoidal signals the shoot-through zero state is applied other state for shoot-through zero state is when the triangle waveform to be less than three sinusoidal signals. Now for detecting these two states we use two *AND* logic gates with three inputs. Three outputs of comparators are connected to three inputs *AND* gate therefore if three inputs *AND* gate be '1' accordingly output *AND* gate is '1' then shoot-through zero state is applied. Fig. 9 shows proposed digital design for pulse generation module maximum boost control.

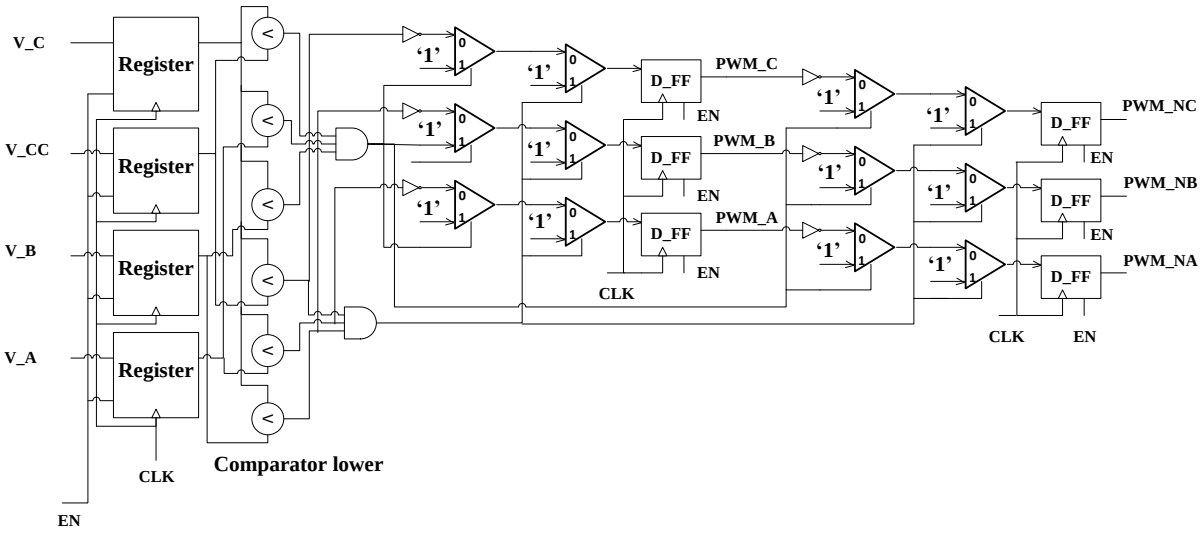

Fig. 9: Proposed digital design for pulse generation module maximum boost control

In this proposed design similar to simple boost control for increase speed and throughput use pipelining technique in proposed maximum boost control pulse generation module, this work is done with applied registers and D Flip_Flops. Fig. 10 shows a total block diagram of proposed fully digital design maximum boost switching on FPGA.

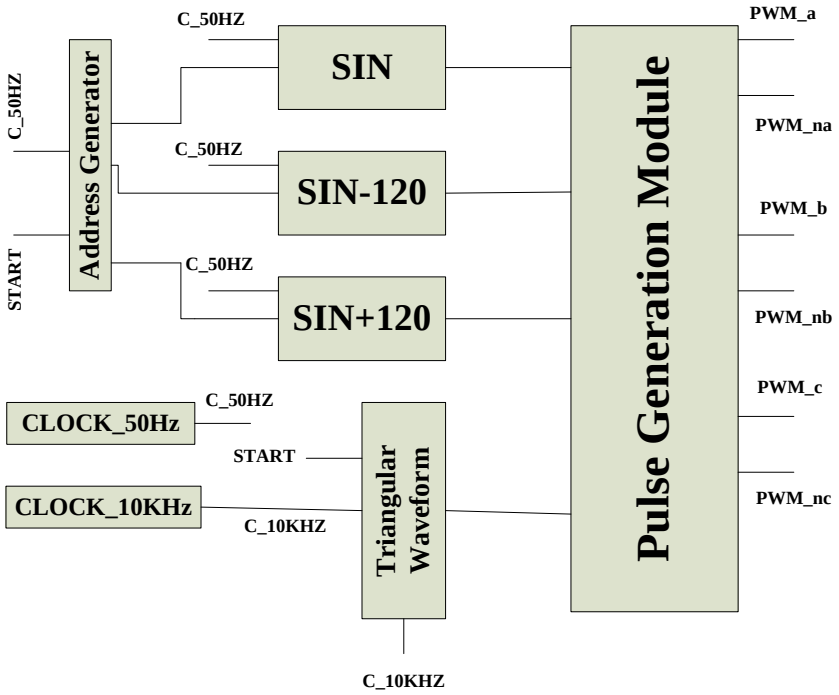

Fig. 10: Total block diagram of proposed digital design maximum boost switching

IV. Comparison and Simulation

We designed a novel optimized and high performance fully digital controller on FPGA for switching control three phases ZSI. The proposed method has best performance hardware and software than conventional methods. The proposed method has been written with VHDL hardware description language. In order to get actual numbers for the hardware usage thus this work was synthesized and implemented using Quartus II 9.1V software, cyclone II FPGA to target device EP2C20F484C6. Also for the verification of the proposed method, we do test and simulation. The Fig. 11 and Fig. 12 shows waveform result of proposed digital design for simple boost control and for maximum boost control.

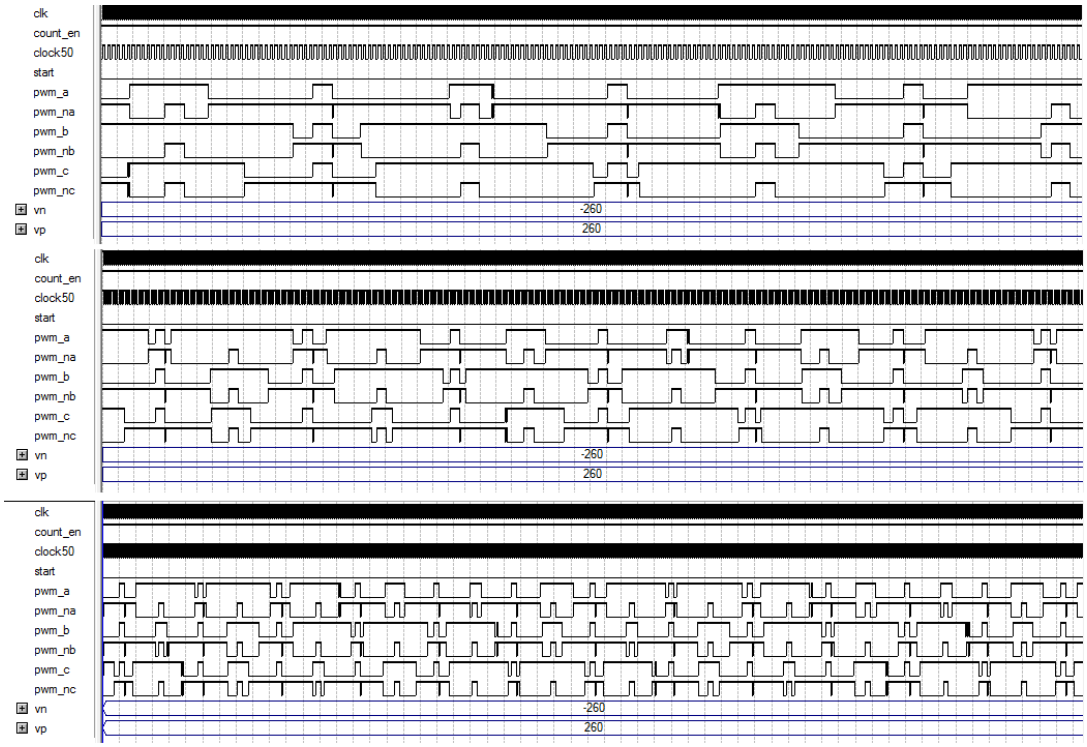

Fig. 11: Waveform of proposed digital design for simple boost control

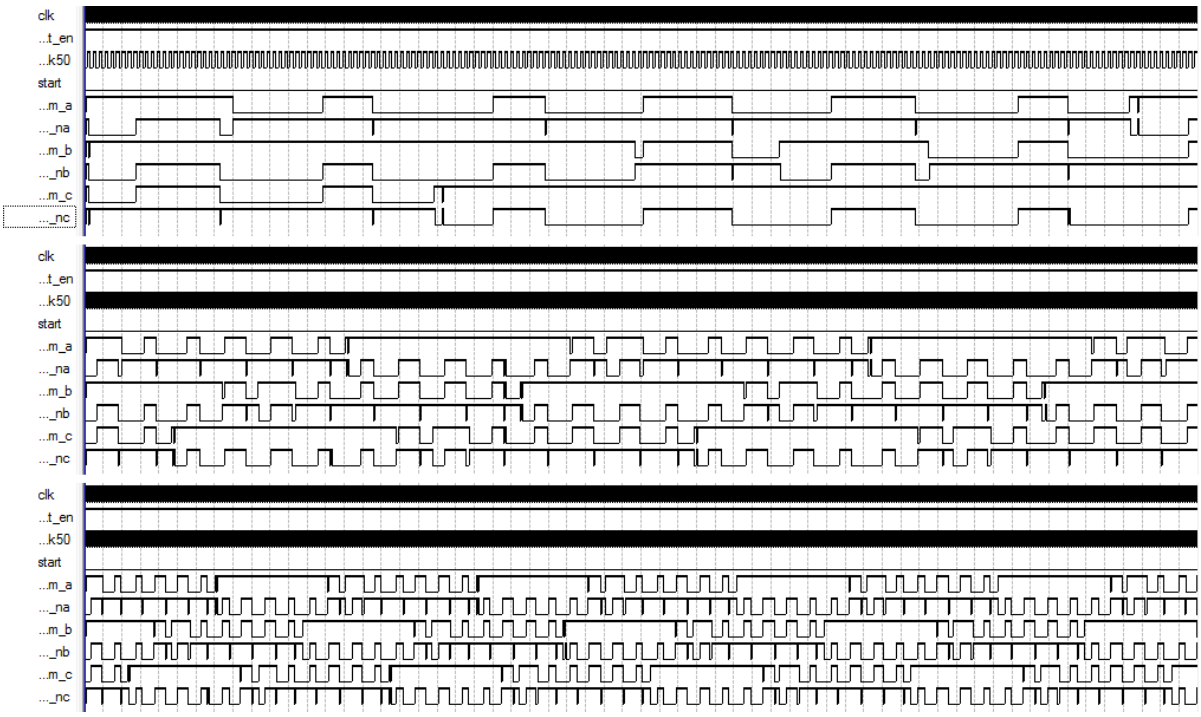

Fig. 12: Waveform of proposed digital design for maximum boost control

Table 1: Utilized hardware on fpga in proposed method

Proposed method	Device	Total logic elements	Total registers	Total memory bits	Max_ Freq (MHz)
Simple boost	EP2C20F484C6	487(%3)	73	10752	241.8
Maximum boost	EP2C20F484C6	398(2%)	73	10752	223.3

Table 1 show utilized hardware on the FPGA and the type of device that has been used in proposed method.

V. Conclusion

The aim of this paper is to develop and implement an FPGA based fully digital controller for ZSI with simple boost control and maximum boost control. The simulation results ensure the feasibility of the high-speed FPGA architecture of the novel proposed digital controller. The advantages of this technique over the others available in the literature include flexibility, high accuracy and reduced area. We first design proposed method based on the fully digital circuit, then implement in FPGA. In this paper, mainly we design and implementation of the digital modified pulse width modulation based on proposed digital circuits for switching control in three phase z-source inverter.

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