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Performance Evaluation of the Loop Buffer Switch Under Prioritized Traffic and Optical Regeneration

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***Abstract*—** In this paper, an all-optical regenerator based, photonic packet switch architecture, which consists of the fiber loop for the storage of the contending packets, is considered. In the loop buffer, the available buffer space may not be fully utilized due to the limited re-circulation count of the data placed on buffer. This limit can be counteracted by placing a pool of regenerators inside the buffer. As optical regenerators are costly devices, hence they should be placed optimally in the buffer. The simulations results are presented by consider Prioritized and non – prioritized traffic. It is shown in the results that regeneration of data is essential if prioritized traffic has to be considered.

***Index Terms*—** TWC (Tunable Wavelength Converters), Optical Packet Switch, Multi-wavelength Buffer, Optical Regenerator, Optical Loop Buffer, Priority

I. Introduction

Optical packet switching (OPS) is a connectionless networking solution that provides very fine granularity and optimum bandwidth utilization, which in a core network can provide very high throughput, data rate transparency and low latency, etc. Still, all-optical switches are difficult to implement, mainly because of unavailability of optical counterparts of electronic RAMs. The one possible choice is, hybrid technology (referred as photonic packet switching (PPS)), which utilizes mature electronics for the control operations and optics for data transmission.

However, the photonic packet switching (PPS), even when applying electronics for control operation, will face the common problems of optical packet switching (OPS) in the data plane, such as the need for fast all-optical switching devices and fast tunable wavelength converters, the lack of optical buffering, etc. Still, PPS is one of the promising technologies. The important aspects of photonic packet switching [1] are packet synchronization, clock recovery, packet routing, control, contention resolution and packet header replacement. This paper deals with the effective utilization of available buffer space in an optical loop buffer based switch architecture. In the optical packet switching, buffering will be required when two or more packets arrive for the same destination in same time slot. One of the contending packets will be directed to the output port, and rests of them, if buffer space is available are stored in fiber delay lines otherwise dropped at the input to the switch. The stored packets can't be stored for infinite duration as the re-circulation count (in case of re-circulating buffer) which arises due to the unwanted constraints such as noise at the amplifier and crosstalk of the components. In the recent past, optical loop buffer based architectures were not paid much attention because of re-circulation limits in-spite of their advantages over other architectures [2]. To counteract the re-circulations problem, we extended the work presented in [3] was extended by employing a pool of 3*R* (re-amplification, re-shaping and re-timing) regenerators inside the buffer [4]. In this paper, simulation result are presented for Prioritized and non – Prioritized traffic, and result shows that the regeneration of data is essential in case of Prioritized traffic.

The paper is organized as follows. In the Sect. 2, overview of the related work is presented. Description of the architecture is explained in Sect. 3, Performance

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measure of the loop buffer based architecture is discussed in Sect. 4. In Sect. 5, simulation results are presented, and finally, Sect. 6 discusses the major conclusions of the paper.

II. Related Works

In the last several years, many research groups all over the world have been involved in the prototype designing of OPS architecture, and this exploration resulted in many architectures. Among the various optical packet switching architectures, the loop buffer based architecture shows inherent advantages over the others [2]. The description of the loop buffer based architectures can be found in [2][3][5][6][7][8] and their comparative study is performed in [2]. It has been found that architecture shown in Figure 1, performs better in comparison to other loop buffer based architectures [2][3][5][6][7][8]. In these architectures, main optical power signal loss is due to the splitter/combiner, which is used to realize the switch architecture. However, the loss of the loop buffer is compensated by optical amplifier to restore the signal's power, but unfortunately, it also adds ASE noise to the signals. In addition to this, crosstalk also occurs among the channels due to the non-perfect spatial isolation of the optical components.

Table 1: List of Symbols Parameters

N	Input/output ports of the switch
B	Buffer space (size of buffer demux /splitter) ($B > N$)
ρ	Load
BL	Average burst length
λ	Wavelength
R	Regenerator
K	Number of re-circulations
A	Physical loss of the switch buffer
G	Gain of EDFA
S	Set
Np	Number of packets
D	Distance

Thus, the system undergoes various distortions due to the impairments caused by noise, attenuation, crosstalk and the fiber dispersion, among others. These degrading terms accumulate in each re-circulation and thus, reduce the SNR. This reduction in SNR, restrict the data storage in the buffer by imposing re-circulation limits (the maximum number of revolution of the data into the buffer before it can be received correctly at the output). However, in the same system, using higher power levels, the number of allowed re-circulations can be increased, but at higher power levels, non-linear effects start to dominate for e.g. the phenomenon of four-wave mixing (FWM) affects the system performance drastically as investigated in [8]. Thus, even higher power levels don't provide very effective solution. In examine the loop, we will find that, in the buffer TWC is one component, which has the potential to suppress the noise and re-generate the signal. However, the commercialized TWC is in its very early stage and is noisy in nature (http://www.inphenix.com). Hence, in the paper, we have assumed that the TWCs are noisy device and only optical regenerators have the capability to re-generate the signal. In past, numerous publications reported on 3R regeneration in the lab environment as well as in field trial [8][9][10][11]. The investigation of 3R regeneration in the fiber loop is performed in [9] with their cascaded effect. The cascade ability of 100 optical 3R regenerators is presented in [8]. In [10], it is shown that, 1,250,000- km transmission is possible through 3R regeneration at 10 GB/s system. Hence, using the 3R regeneration mechanism inside the buffer, the performance of the switch can be improved significantly.

A regenerator based OPS architecture is proposed by [8]. However, in this architecture data is taken out from the loop buffer, electronically regenerated and then again, pushed into the loop after electronic-to-optical (E/O) conversion. So in this process optical-to-electronic (O/E) and E/O conversion is required. The major advantages of architecture consider in this paper over the architecture [8] is:

1. Simultaneous read/write operation can be performed.
2. Control unit complexity is less (as in the architecture, A1 there are fewer control point).
3. No O/E and E/O conversion.
4. Buffer usage is better [3], in comparison to other loop buffers based architecture.

III. Loop Buffer Based Architecture

In this section, the loop buffers based architecture structure without and with regeneration are discussed. This section highlights architecture A1 and architecture A2 with advantage of architecture A2 over architecture A1.

3.1 Architecture A1

The architecture A1 is shown in Figure 1. Here, buffered packets use WDM technology to share the loop buffer [1]. The numbers of buffer wavelengths depend on the desired traffic throughput, packet loss probability and various component parameters. In this architecture, at the input to the switch, the wavelengths of the incoming packets are tuned appropriately, either to place them in the buffer or to direct them to their respective outputs. The incoming packets can be placed on the loop buffer by converting their wavelengths to the available free buffer wavelengths; and if the buffer is full then the packets cannot be stored. In such a case, packets will be dropped at the input to the switch and are considered as lost. The buffered packets will keep on circulating around the fiber loop until contention resolves. Afterwards, the packets can be read out from

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the buffer by tuning their wavelengths appropriately (through buffer TWCs) by following the routing pattern of output demux.

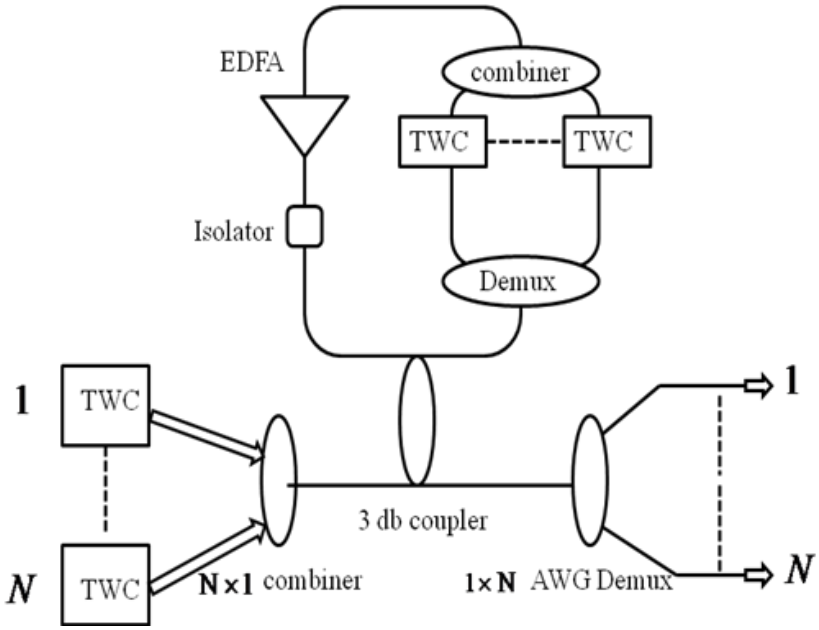

Fig. 1: Schematic of the architecture A1

The switch uses (B + N) wavelengths, in which N wavelengths are used for the direct transfer of packets and rest B wavelengths are used for the buffering of packets. Let S_N and S_B are the sets of wavelengths used for the direct transfer and buffering of packets. Equivalently, we can define, $S_N = \lambda_1^0, ..., \lambda_N^0$ and $S_B = \lambda_1^b, ..., \lambda_B^b$ such that $S_N \cap S_B = \phi$ as the allowed range of both the demux (output and buffer) are different. Hence, the buffer demux allows only S_B wavelengths to pass through it and blocks other S_N wavelengths, and output demux do the vice versa. Therefore, once wavelength of the incoming packet is assigned by the input TWC, it will either be directed towards buffer or to the receptive output. Similarly, packet placed in the buffer at wavelength λ_i^b (where $\lambda_i^b \in S_B$) can be read out from the buffer by tuning its wavelength $\lambda^0{}_j$ (where $\lambda^o{}_j \in S_N$) by respective buffer TWC. Hence, switching of the packets takes place in wavelength domain.

The main limitations of the architecture are found as under.

1. It has less buffer utilization due to re-circulation count.
2. The packet loss probability of low priority packet is very higher, due to the higher loss of packet.
3. Higher priority packet captures the full buffer capacity.
4. The performance of the switch degrades severely due to the re-circulation count.

3.2 Architecture A2

The modified architecture consists of N tunable wavelength converters (TWCs) one at each input, a re-circulating loop buffer and one 1 × N demux at the output of the switch (Figure 2). The re-circulating loop comprises of 3dB coupler, demux, TWC, regenerator (denoted by R), combiner, EDFA to compensate the loop loss and an isolator in Figure 2, R+TWC denotes that in corresponding branch of buffer demux, both regenerator and TWC are placed. Hence, in the architecture A1, we have added optical regenerators in a few branches of buffer demux, and placing of regenerators is done in such a way that each packet gets regenerated before it crosses the upper circulation limit by any one of the regenerator. The elaborated discussion as follows:

The buffer demux have B ports correspond to wavelengths ranging from λ_i^b to λ_B^b (Figure 3), and on a few of these wavelengths regenerators are placed. In each pass through the buffer TWC wavelength of each packet say λ_i^b, for $2 \le i \le B$, gets shifted to its lower adjacent wavelength $\lambda^b{}_{i-1}$ (Figure 4a) or converted to intended output port wavelength $(\lambda^o{}_j)$

(Figure 4b). As shown in the Figure 3, in the slot '*i*' the wavelength λ^b_i gets shifted to wavelength λ^b_{i-1}, in the slot '$i+1$', the wavelength λ^b_{i-1} gets shifted to wavelength λ^b_{i-2} and so on. If packet stays in the buffer, then due to the wavelength shift, packets will pass through the each port of the buffer demux, and as on some of these ports regenerators are placed. Hence, packets will automatically pass through the different regenerators. In this process, few packets which do not require regeneration will also get regenerated, but there is no harm if a packet gets regenerated earlier than it reaches the maximum circulation count.

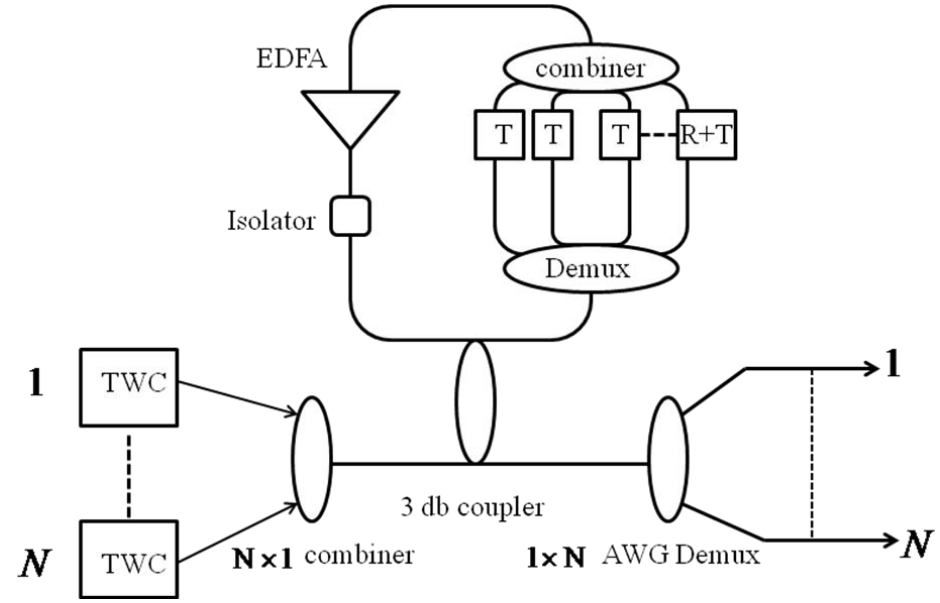

Fig. 2: Schematic of the architecture A2 (R-Regenerator)

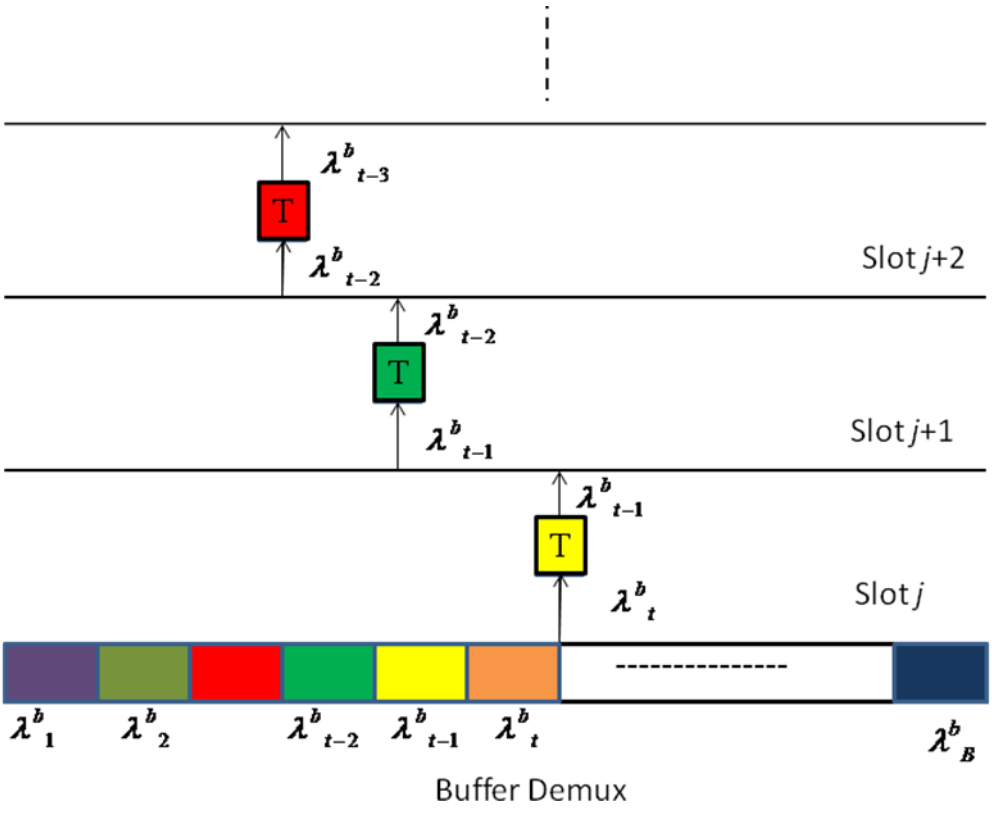

Fig. 3: Schematic of the wavelength shifting through buffer TWC

This shifting in wavelength may eventually bring a packet to the wavelength λ^b_1 and to maintain FIFO, wavelength of this packet can again be converted to λ^b_B or any other wavelength decided by the 'tail' (t) of the particular queue. Thus, the packets stored in the buffer follow the cyclic nature of the wavelength conversion process (Figure 5).

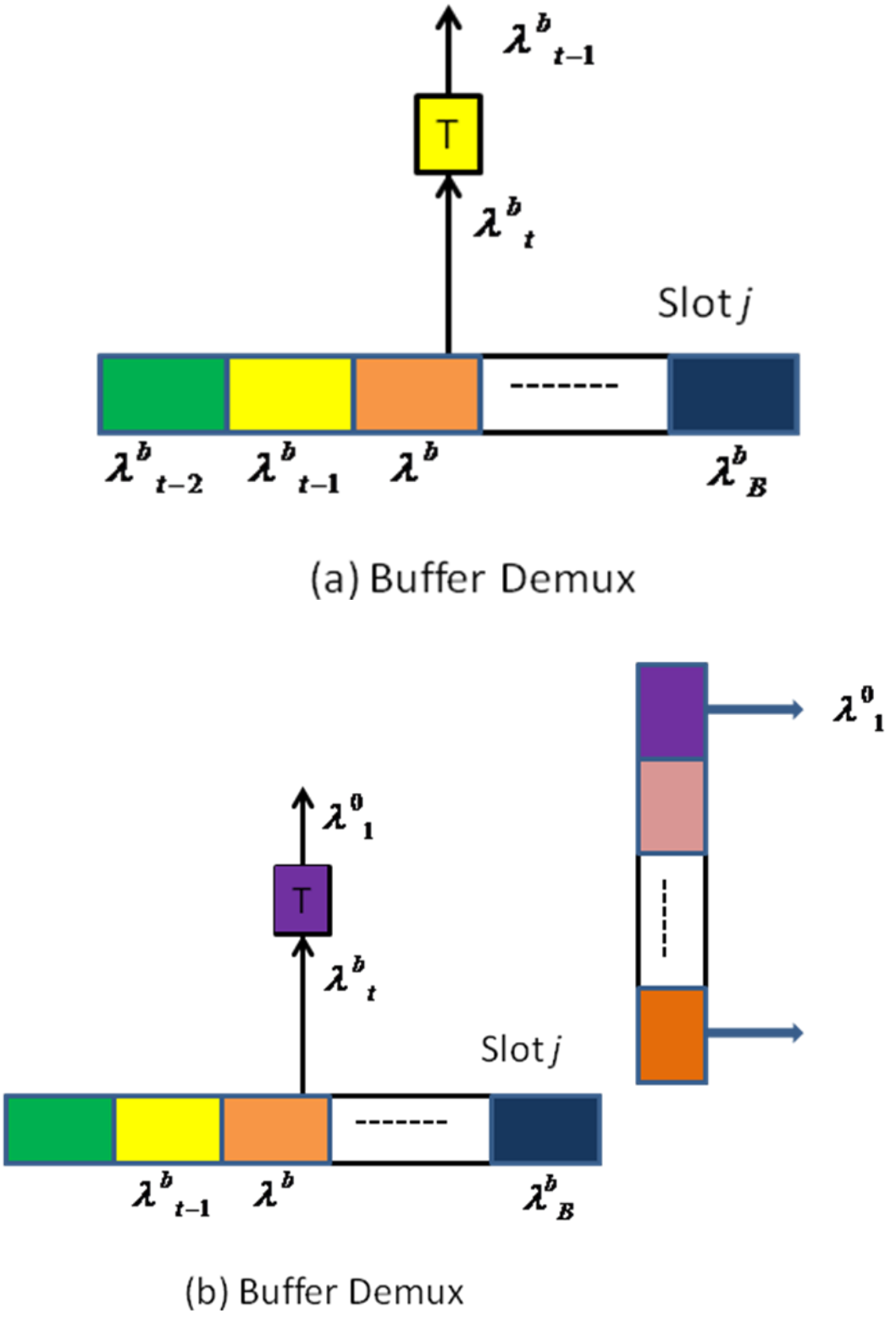

Fig. 4: Schematic of the (a) wavelength shifting through buffer TWC, (b) output wavelength tuning through buffer TWC

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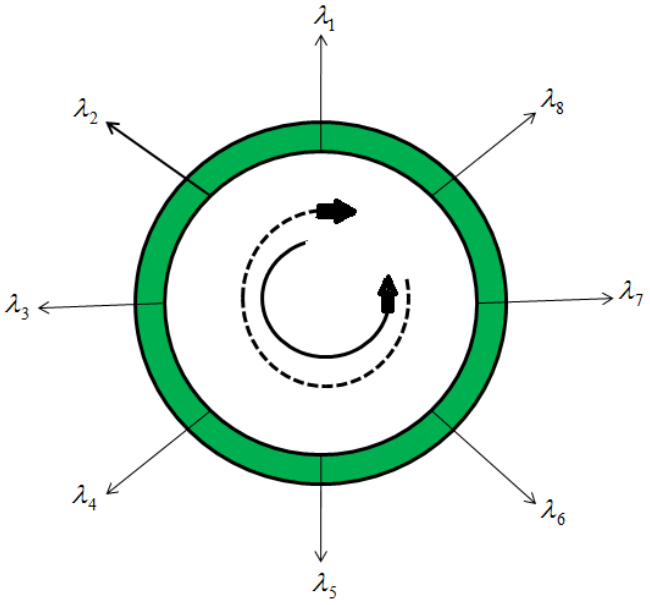

Fig. 5: Schematic of the cyclic nature of the 8 wavelengths buffer, (solid line—wavelength filling in buffer and dotted line—wavelength shifting)

3.3 Advantages in Architecture A2 over Architecture A1

The main advantages gained due to the placement of the regenerators are:

1. Signal quality will be maintained.
2. Buffer capacity can be utilized effectively.
3. The regeneration of signals will allow the cascadability of the switches in the core network.

In the next sub section, regenerated based switch architecture is considered.

And it is shown, the circulation limited can be overcome by placing a regeneration scheme inside the buffer. Hence, it is exceeded that, the performance of the switch should improve significantly.

IV. Performance Measures of the Loop Buffer Based Architecture

The design of any optical packet switch architecture is affected by nearly countless attributes. However, the most important one are described in Table 1. The performance of the switch in terms of loss, power, noise and BER analysis is performed in [12]. In the same paper, the detrimental effect of four-wave mixing (FWM) is also studied, and it is concluded that the architecture shown in figure 1, suffers from the re-circulation limits. Hence, to enhance the re-circulation count the placement of the regenerators inside the buffer is proposed in [4] [13].

The resultant architecture is shown in Figure 2, here 'R' represents the regenerators and 'T' represents the tunable wavelength converter. This regeneration will be essential part of the loop buffer under prioritized traffic as a few low priorities may stay in the buffer for more than B re-circulations or in other words may stay in the buffer for more than B slots. The required number of regenerators for different re-circulation limit and buffering capacity can be obtained from [4] such that

$$R_{\min} \geq \left\lceil \frac{B}{K} \right\rceil - \quad if \quad \frac{B}{K} \neq I \tag{1}$$

$$R_{\min} > \frac{B}{K} - 1 \quad if \quad \frac{B}{K} = I \tag{2}$$

full buffer capacity can be utilized without any recirculation limit. In the loop buffer, all-optical 3R regeneration is assumed.

Table 2: Critical Attribute and Their Affect

Attribute	Effect	Reference
Attenuation	Scaling become Critical	[7]
Dispersion	Bit Rate gets limited	[8]
ASE Noise	Number of re-circulation gets reduced	[8]
FWM	Number of re-circulation gets reduced	[8]

Table 3: Performance Evaluation under Various Attributes

Performance Measure	Reference
Loss power ,noise and BER analysis	[8]
Affect of FWM	[8]
Placement of Regenerators	[10]
Packet Loss Probability(Without Re-circulation limits)	[12]
Packet Loss Probability(With Re-circulation limits)	[13]
Packet Loss Probability(In presence of Regenerators)	[13]

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Hence, in turns it can be further assume that after regeneration a packet can re-circulate for *MC* more recirculation. Therefore, multiple regenerations of packets will allow longer duration of the data storage [4].

V. Simulation and Result

The performance evaluation of the switch is measured in forms of packet loss probability. The simulation is done MATLAB. The SIMULATOR is the random event generator. Hence, to observe the steady state performance result Monte-Carlo simulation is performed. The simulation is performed for 2×10^6 iteration.

5.1 The Traffic Model

In this paper random traffic model is considered. This model is simple; still it provides good insight into the performance of the architecture, and also help us to compare our result with previous publish results [7].

This model assumes that the packet can arrive at any of the inputs with probability *P* and each packet is equally likely to be destined to any of the *N* outputs with probability *1/N*. Thus, the probability that *Z* packets arrive for a particular output in any time slot is given by [14].

$$P_r(z)=\frac{N!}{(N-z)!z!}\left(\frac{P}{N}\right)^z\left(1-\frac{P}{N}\right)^{N-z} \quad (3)$$

In case of traffic with different class or priority, if $Q_1,Q_2,.....,Q_s$ denote the ratio *class-1, class-2, class-S* packets to the total number of packets; where *S* is the number of priority classes (*1* is the highest, *S* is the lowest). Probability that n_1 *class-1*, n_2 *class-2*... n_s *class-S* packets arrive at the switch in a same time slot, is given by:

$$b_{n_1,n_2,...,n_s}=P_r\sum\nolimits_z(Q_1)^{n1}(Q_2)^{n2}.....(Q)^{ns}\frac{\sum_z(n_z)!}{\prod_z(n_z!)} \quad (4)$$

Where $Q_1,Q_2,.....,Q_s$ mean the ratio of *class-1, class2… class-S* packets to the total number of packets.

5.2 Wavelength Consideration and Conversion

For the switch architecture the algorithm according to which the packets are forwarded to the output or stored into the buffer, is as follows.

The switch uses (*B+N*) wavelengths, where *B* is the number of buffer wavelengths, and *N* is the number of wavelengths used for direct transmission to the output by passing the fiber loop. The steps to be followed are:

1) All-optical wavelength converters at the inputs of the switch can be tuned to any of the (*B+N*) wavelengths instantaneously.

2) The buffer is such that read and write operations happen simultaneously in the same slot for the loop buffer wavelength.

5.2.1 Traffic without Priority without Re-circulation Limits

1. If there are $i(1\le i\le B)$ packets in the buffer for the output *j*, only one of i packets will be sent to the output *j*. if in the same slot, there are one or more packets also present at the inputs for the output *j*, then these will be buffered in the loop buffer to the extent allowed by rules 3 and 4. If all the buffer wavelengths are occupied, then remaining packets will be dropped.

2. Considering the case when there is no packet in the buffer to the output *j*, but *m* input lines have packets for that output, and then one of these *m* packets is directly sent to the output *j* in the switch. The remaining *m-1* packets will be stored into the buffer to the extent permitted by rules 3 and 4.

3. The number of packets X_j in the buffer for the output *j* should never be greater than *B*, i.e. $X_j\le B$ for *j =1* to *N*.

4. The total number of buffer space used should never exceed *B*, i.e. $\sum X_j\le B$ .Through out the paper in the simulation, the size of switch is assumed to be 4×4.

In Figure 6 packet loss probability vs. load is plotted with buffering capacity of 4, 6, 8 and 16, with load varying from 0.2 to 1 and traffic is without any priority. It can be clearly observed from the figure that for the 4×4 switch, *B* = 8 is the acceptable switch configuration. For *B* = 8 the packet loss probability for the lower loads (less than 0.5) is below 10^{-6}. at the load of 0.6 for *B* = 8, the packet loss probability is below 10^{-4}, whereas for *B* = 4 it is closer to 10^{-2}. Hence, *B* = 4 can be considered as very small buffer space. For *B* = 16, the packet loss probability is 10^{-4} even at the load of 0.8. It means as load increases, to maintain the same packet loss probability, more buffer space is required.

5.2.1.1 With Re-Circulation Limits

The algorithm is same as above, except the third point will be replaced as,

1. The number of packets X_j in the buffer for the output *j* should never be greater than min (*MC*, *B*), i.e. $X_j \leq \min(MC, B)$ for *j* = 1 to *N*. where *MC* is maximum recirculation limit.

The Figure 7 shows the packet loss probability of the switch architecture for the different circulation limits in the loop buffer with buffering capacity of *B* = 8. Curves are plotted for the maximum circulation limit values (*MC*) of 2, 4, 6 and 8. We can clearly visualize that as the maximum number of allowed re-circulation increases, the probability of packet loss decreases. At the load value 0.6, it can be observed for *MC* = 2, packet loss probability is above 10^{-2}, for *MC* = 4 it is above 10^{-3}, so improvement by a factor of more than 10. It shows that the switch architecture give improved performance as we relax (increase) the number of maximum circulation limit. The nearer the circulation limit is to total buffer capacity, the more improved performance it provides. As we can see at load 0.6, for *MC* = 8 the packet loss probability is 10^{-4}, which is under acceptable limits. This happens because in case of *MC* = 2, buffer space may not be fully utilized due to circulation limit even if buffer space is available, we cannot store more than two packets for each output. So if there are more than three packets at the inputs of the switch in single time slot, except three all other packets have to be dropped. As we increase the circulation limit, the buffer capacity can be utilized more effectively. It proves from the fact that the curve for *MC* = 8 in Figure 7 resembles the curve for *B* = 8 in Figure 6. It can be inferred that when circulation limit comes closer to the total buffer size, the behavior of the architecture is similar to its behavior with buffer having no circulation limit.

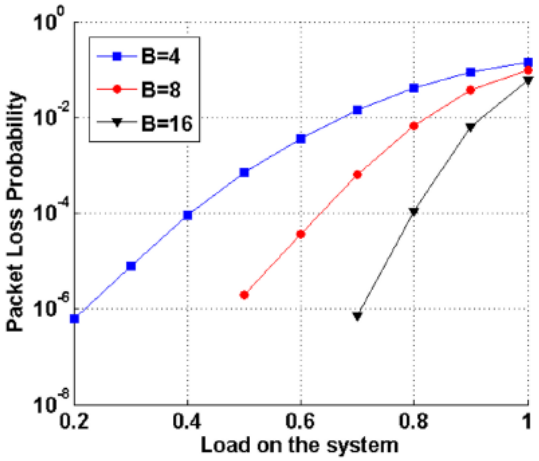

Fig. 6: Packet loss probability vs load for different buffer space

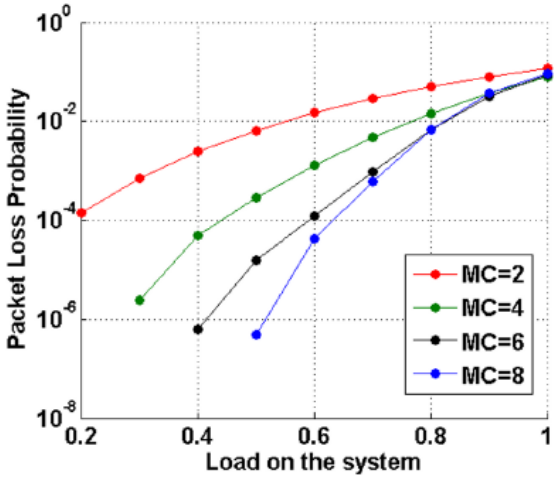

Fig.7: Packet loss probability versus load under different re-circulation limits

5.2.2 Traffic with Priority (Without re-circulation Limits)

1) In any slot, if there are one or more packets present in the buffer or in the input lines for output *j*, then the packet would be sent to the output *j* following the rules 2 and 3.After repeating rule 2 and 3 for each output, remaining packets in the input lines would be buffered following rule 5-6. Any leftover packets will be dropped.

2) If there are only two classes (priority) of packets namely high and low and there are packets in the buffer for the output *j*. If high priority packets are in buffer for output *j*, send one of them to the output *j*. If no high priority packet is present in the buffer for output *j*, then in that slot check all inputs of the switch for a high priority packet for the output *j* and if one or more high priority packets are present in the input for output *j*, send one of them to the output *j*. if no high priority packet is sent to output *j*, go to rule 5.

3) If there is no high priority packet for output *j*, neither in buffer nor in input lines, then if there are low priority packets present in the buffer for output *j*, send one of them to the output *j*. And if there is no (neither high nor low) packet in the buffer for the output *j* and no high priority packet in input lines for output *j* in that slot, then in that slot check inputs of the switch for a low priority packet for the output *j* and if one or more low priority packets are present in the input for output *j*, send one of them to the output *j*.

4) After applying rule 2-3 for each output, first check for high priority packets in the input lines for any output and buffer them to the extent rule 5 and 6 allows. If all the high priority packets in the input lines are buffered, then send the remaining low priority packets to the buffer following rule 2 and 3.

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5) The number of packets X_j in the buffer for the output j should never be greater than B, i.e. $X_j \le B$ for j = 1 to N.

6) The total number of buffer space used should never exceed B, i.e. $\sum X_j \le B$.

In the first simulation as shown in Figure 8 there are 50% high priority traffic and 50% low priority traffic of the total traffic the factor Q can be defined as:

$$Q = \frac{HPP}{HPP + LPP} = \frac{HPP}{TP} \quad (5)$$

Where,

HPP=High Priority Packets

LPP=Low Priority Packets

TP=Total Packets

The buffer size is B = 8. It can be observed from Figure 8 that switch efficiently stores the high priority traffic. High priority packet loss probability at load 0.6 is below 10^{-6}, which is almost negligible. At traffic load of 0.7, high priority packet loss probability is approximately 10^{-5} and low priority packet loss probability is nearly 10^{-3}. It can be inferred that the switch can provides better quality of service to high priority packets than low priority packets. The total packet loss probability matches exactly with the packet loss probability for traffic with no priority (Figure 8). So, the switch is giving good performance for high priority traffic without much deteriorating performance for the low priority traffic as they have low priority and loss of some of them can be afforded.

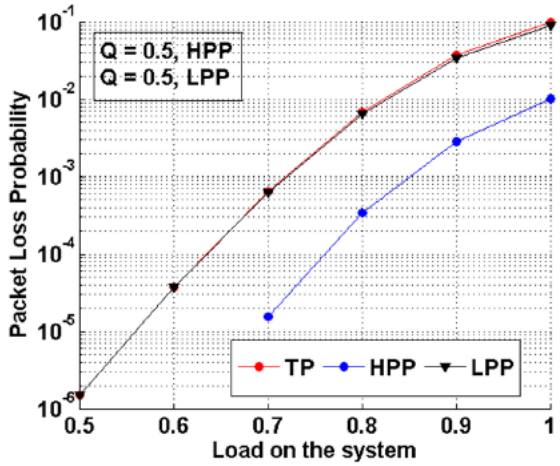

Fig. 8: Packet loss probability versus load on the system for high priority and low priority

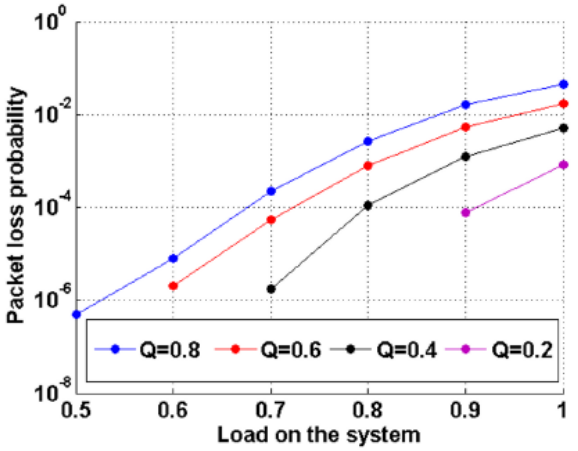

Fig.9: Packet loss probability versus load on the system for varying high priority traffic load for N= 4, B = 8

In Figure 9, comparison has been made between high priority traffic, here Q = 0.2 signifies that in total traffic, 20% is high priority traffic and 80% is low priority traffic. As we reduce the high priority packets from the total traffic, the packet loss probability reduces. Up to the load of 0.7, the high priority packet loss probability is around 10^{-4}.In Figure 10, it can be observed that for the different percentage of low priority traffics, the switch performance is almost same. It is expected as low priority packets will always be lost over high priority packets. In Figure 11, low priority traffic is 70% of the total traffic. Packet loss probability for low priority traffic is same as for the traffic with no priority.

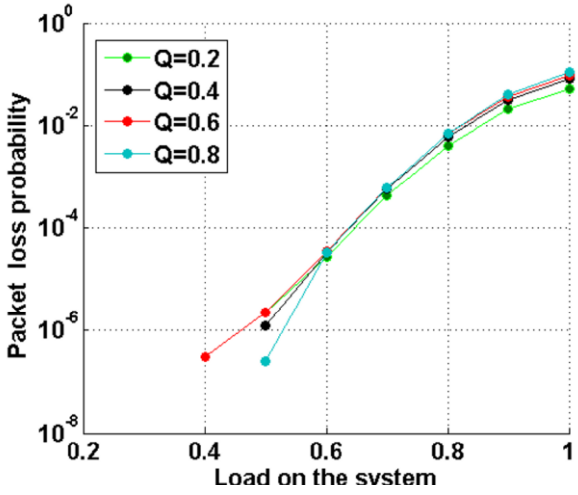

Fig. 10: Packet loss probability versus load on the system for varying low Priority traffic load for N = 4, B = 8.

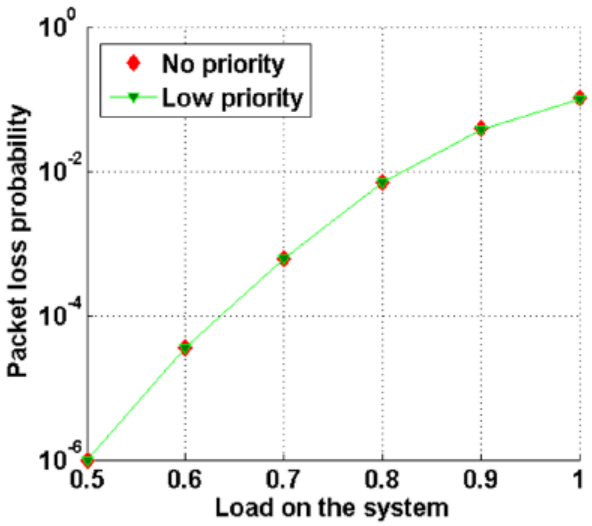

Fig.11: Packet loss probability versus load on the system for N = 4, B= 8 for without priority and low priority traffic (70% of total traffic)

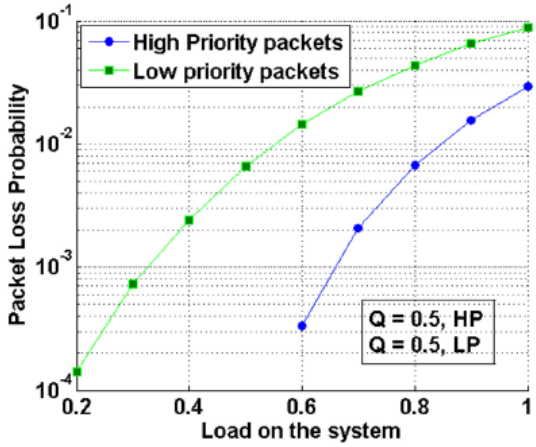

Fig. 12: Comparison of packet loss probability versus load on the system between high and low priority packets for N = 4, B = 8 and *MC* = 2

5.2.2.1 With Re-circulation Limits

The algorithm is same as above, except the fifth point will be replaced as,

1) The number of packets X_j in the buffer for the output *j* should never be greater than min (*MC*, *B*), i.e. $X_j \le \min(MC, B)$ for *j* = 1 to *N*. where *MC* is maximum recirculation limit.

From Figure 12 to Figure 14, packet loss probability versus load on the system is plotted for the traffic with priority for different circulation limits in the loop buffer. In Figure 12, the circulation limit (*MC*) is two. At load 0.6, high priority packet loss probability is above 10^{-4}, whereas low priority packet loss probability is above 10^{-2}. It is because high priority packet is always saved from being lost at the cost of low priority packets. Figure 13 shows the results for *MC* = 4, which shows improvement in the packet loss probability for both types of priorities packets in comparison to *MC* = 2. The packet loss probability of high priority packets at load 0.6 is below 10^{-4}. The improvement is because the more number of packets can be stored inside the buffer due to relaxation in circulation limit. Figure 13 and Figure 14 show the results for *MC* = 4 and *MC* = 8, respectively. As we move from *MC* = 4 to *MC* = 8, the improvement in the performance of the switch for high priority packets is more than for low priority packets. As at the load 0.7, in Figure 13 the high priority packet loss probability is 6×10^{-4}, and in Figure 14 it is 2×10^{-5}. At the same load in Figure 13 (for *MC* = 4) the low priority packet loss probability is 10^{-3} and in Figure 14 (*MC* = 8) it is 8×10^{-5}. It is because; relaxation in circulation limit allows more number of high priority packets to be stored in comparison to low priority packets if buffer space is available. From all the above four figures, it can be observed that the algorithm of the switch provides better quality of service to high priority packets than low priority packets for any circulation limit. However, as the circulation limit increases, improvement in performance occurs for both types of priorities. In the next two figures (Figure 15 and Figure 16), we can observed the effect of circulation limit on

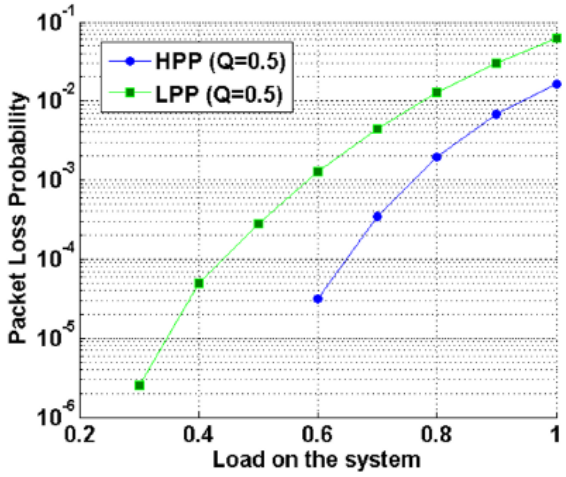

Fig.13: Comparison of packet loss probability versus load on the system between high and low priority packets for N = 4, B = 8 and *MC* = 4

high priority packets and low priority packets, separately. The Figure 15 is also for the switch of size 4×4, with the buffer size of *B* = 8, for the values of maximum circulation limits *MC* = 2, 4, 6 and 8. The traffic considered is uniformly distributed random traffic with high packet priority packets are 50% of the total traffic. Figure 15 shows the packet loss probability

for the traffic with high priority for different values of *MC*. In the simulation, the high priority traffic is 50% of the total traffic. From the Figure 15, it can be visualized that, as we increase the circulation limit *MC*, the packet loss probability decreases quite significantly. At load 0.7, for *MC* = 2, the packet loss probability is above 10^{-3}, for *MC* = 4 it is 6×10^{-4}, and for *MC* = 8, the packet loss probability is 2×10^{-5}.We can observe that the switch performs quite efficiently for high priority packets. At the higher loads on the system, for *MC* = 4 and 8, the packet loss probabilities are nearly same. It is because at higher loads, buffer space gets occupied quite frequently; and more number of packets gets lost at the input of the switch. Figure 16 shows the packet loss probability for the traffic with low priority for different values of *MC*. In the simulation, the low priority traffic is 50% of the total traffic. From the Figure 16, it can be visualized that as we increase the circulation limit *MC*, the packet loss probability decreases quite significantly. At load 0.6, for *MC* = 2, the packet loss probability is above 10^{-2} for *MC* = 4 it is almost 10^{-3}, and for *MC* = 8, the packet loss probability is 6×10^{-2}. Every time, as we relax the *MC*, we see an improvement of factor 10 except for *MC* = 8. Reason for the less improvement for *MC* = 8 is same as explained in previous paragraph. If the loop buffer has circulation limits of two or four and *B* = 8, then a large buffer space may remain efficiently unutilized, because as only two (for *MC* = 2) or four (for *MC* = 4) can be stored in the buffer. Hence, if for a particular output port more than *MC*, say *MC*', packets arrive then *MC'*-*MC* packets have to be dropped even if some buffer space is vacant. There must be some provision inside the buffer which can remove the effect of circulation limit so that buffer space can be utilized efficiently. Circulation limit inside the buffer has deleterious effects on the performance of loop buffer based switch architecture. It leads to losing of packets in spite of free buffer space. The next section of the paper addresses this issue and it discusses about removal of circulation limit using regenerators inside the buffer.

5.2.3 Performance analysis of switch (circulation limit in the buffer)

In photonic packet switches, the storage duration of the packets in the fiber delay-line is limited by the number of recirculation allowed in the buffer. When more than one packet arrives for the same output in a single time slot, one of them will be sent to the output. In case of class differentiation, high priority packets would be given preference. If possible, other packets would be stored in the buffer. The packet with higher priority will be stored first then if buffer is vacant, then lower priority packets will also be stored. Now if buffer allows finite amount of circulations to a packet i.e. *MC*, any packet can stay only for *MC* circulations inside the buffer. If, for any output, there are *MC* packets inside the buffer, the next packet to be stored in the buffer for the same output will take more than *MC* circulations before coming out of buffer, hence it should be dropped because it will be degraded much inside the buffer because various impairments like *ASE*, crosstalk etc. and cannot be retrieved at the outputs. If there are *m* packets already stored in the buffer for the same output, then the next packet for the same output to be stored in the buffer will have to circulate at least *m+1* times (may be more in case of prioritized traffic) in the buffer before being sent to the output. Therefore, in prioritized traffic a packet may re-circulate for more than B re-circulations and hence, regeneration of data is essential in the loop buffer. As in the absence of regeneration, packet will not be able to survive more than few re-circulations due to the accumulated impairments.

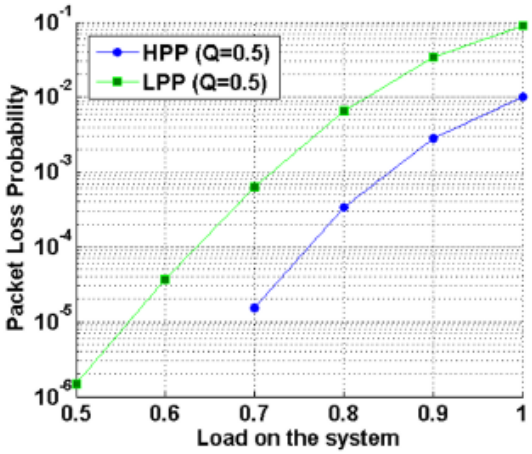

Fig. 14: Comparison of packet loss probability versus load on the system between high and low priority packets for N = 4, B = 8 and MC = 8.

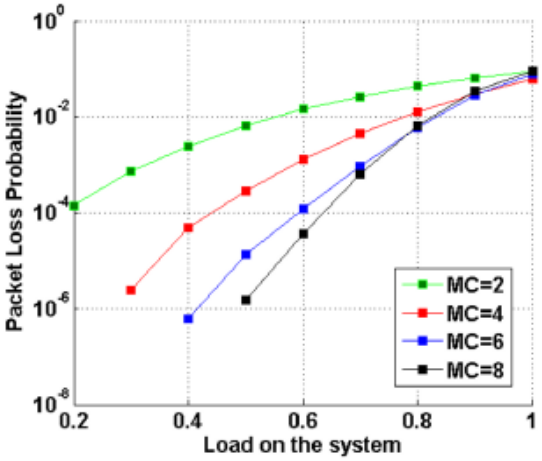

Fig. 15: Packet loss probability versus load on the system for the traffic with high priority for different MCs, N=4, B=8.

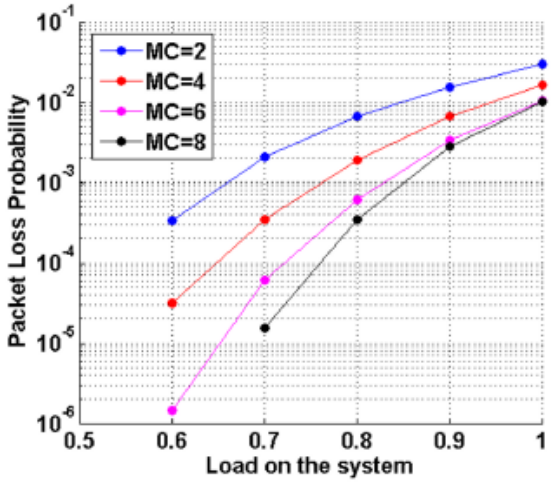

Fig. 16: Packet loss probability versus load on the system for the traffic with low priority for different *MC*s, N=4, B=8.

5.2.4 Algorithm of the Switch under Regeneration

The algorithms of the switch is same as traffic without priority with re-circulation limit except,

1) If the number of packets in the buffer is less than *MC*, and the packets in the input lines to the output j are to be buffered, they would be stored. And if the number of packets in the buffer is equal to *MC*, then check if the packet in the input for output j would be able to get a regenerator in any circulation before crossing *MC*. If yes, then packet must be stored in the buffer, if rule-2 allows it.

2) If the packet has to be stored for more than one regeneration, then it will be buffered in the loop only if regenerator is available in the particular slots in which regeneration is needed.

In this sub-section the performance of the switch is measured, while varying the number of regenerators present in the buffer. In the simulation *MC*= 2 and 4 is considered.

Circulation Limit (MC = 2)

The required number of regenerators for the buffer with maximum re-circulation limit (*MC*) two is four. In Figure 17, packet loss probability has been obtained for different numbers of regenerators (*R*) ranges from 0 to 4, for the switch size is $N = 4$ and buffer size $B = 8$. $R = 0$ implies that inside the buffer there is no regenerator, the corresponding packet loss probability curve shown in Figure 17 and it resembles with the performance of the switch for *MC* = 2 without any priority. It can be observed that for traffic load of 0.6, the packet loss probability is above 10^{-2}, which is below acceptable performance level. At the traffic load of 0.6, for single regenerator ($R = 1$), the improvement in performance is minuscule, and values are 10^{-2} and 2×10^{-2} for $R = 0$ and $R = 1$ respectively. But as we put second regenerator ($R = 2$) in place, the performance improves significantly, with packet loss probability value reduces to less than 10^{-3} and the improvement by a factor of more than 10. Furthermore, increasing number of regenerators from two to three ($R = 3$), improvement is not very significant as compared to the improvement occurred in case of from $R = 1$ to $R = 2$. In case of $R = 2$ to $R = 3$, value of packet loss probability reduces only from 9×10^{-4} to 7×10^{-4}. But again, by increasing number of regenerators from 3 to 4, we get an improvement of a factor more than 10, as respective values are 7×10^{-4} and 2×10^{-5}. It can be observed in the Figure 17 that there is a difference in packet loss probability up to load of 0.7 and becomes nearly equal from the load 0.8, because after load 0.8, a large number of packets arrive and even large buffer space cannot improve packet loss probability. For $R = 4$, at the traffic load 0.6, the packet loss probability is below to 10^{-4} so, placing four regenerators inside the buffer makes it free of the circulation limit. Since, regenerator's cost is high, it is better to use those many regenerators, which is cost effective and at the same time they can offer good performance. In case of buffer with maximum circulation limit (*MC*) two, number of regenerators two and four are more effective and logical. It means it is better to use two regenerators instead of three as the improvement in performance (packet loss probability) is not much when we increase number of regenerators from two to three, and cost is increased as regenerators are costly.

Circulation limit (MC = 4)

For $N = 4$ and $B = 8$ with maximum circulation limit of the buffer is *MC* =4, number of regenerators required to utilize the buffer capacity effectively is two ($R = 2$). In Figure 18, packet loss probability with respect to load on the system is given for different number of regenerators ($R = 0$ to 2).When there is no regenerator ($R = 0$), at modest load of 0.6, which is quite relevant in real time scenario, packet loss probability is 10^{-3}. By placing one regenerator ($R = 1$) inside buffer, packet loss probability improves significantly. The packet loss probability is in between 10^{-4} and 4×10^{-5}. Hence, Improvement is by a factor more than 10. There is very little difference in packet loss probability values for $R = 1$ and $R = 2$, at the traffic load 0.6, after that for load 0.7 and above, the values are nearly same. For *MC* = 4, only one regenerator can give satisfactory performance.

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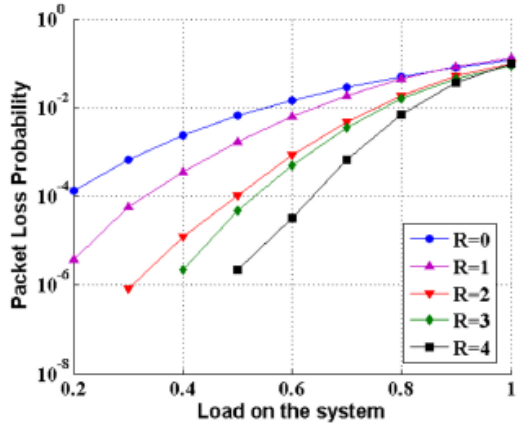

Fig. 17: Packet loss probability v/s load on the system with different number of regenerators for N = 4, B = 8, MC = 2 under random traffic conditions

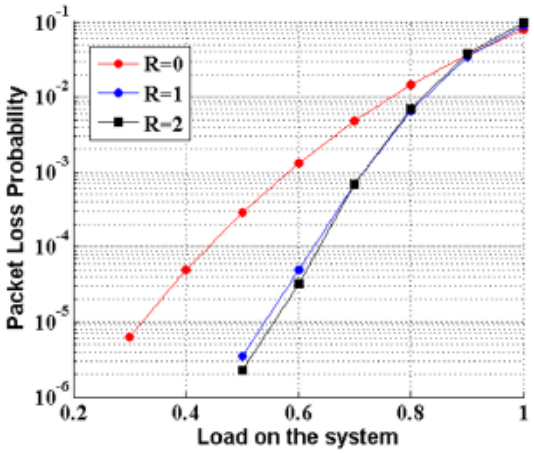

Fig. 18: Packet loss probability v/s load on the system with different number of regenerators for N = 4, B = 8, MC = 4 under random traffic conditions

VI. Conclusions

Quality of service is an important issue for the real time applications. Loss of information should be avoided as it will lead to unintelligible information. There is always distinction between applications on the basis of priority. Some of them are highly prioritized. They must be provided better quality of service. Loop buffer based switch architecture (A2) provides better quality of service to the high-priority data. At the same time it does not degrade the quality of service for the low priority traffic. Circulation limit inside the buffer has deleterious effects of the performance of loop buffer based switch architecture. It leads to lose of packets in spite of free buffer space. The re- circulation of circulation limit can be overcome by placing regenerators inside the buffer. This has been shown that using regenerators inside the buffer circulation limits can be relaxed, and full buffer capacity can be utilized without any circulation limits. All-optical regenerators are preferable over optoelectronic regenerators, due to the lesser speed of opto-electronic components to their electronic counterparts. The cost of the regenerator will affect the cost of the switch, so the number of regenerators should be less in the number is placed according to the required performance of the switch.

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