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Fredkin Circuit in Nanoscale: A Multilayer Approach

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***Abstract*—**Nanotechnologies, exceedingly Quantum-dot Cellular Automata (QCA), presents a notable perception for upcoming nanocomputing. Feature extent of circuits is moving to sub-micron point that produces the sophisticated device intricacies. In this work, QCA is considered as an application technique for reversible logic. A multi-layer reversible Fredkin circuit is proposed with QCA nanotechnology. The accomplishment of the outlined circuit is substantiated with five existing Fredkin gate, which exhibits from 71.20% to 37.50% improvement in term of cell intricacy. The proposed design uses 55 cells concerning only 0.03 μm^2 area and latency is 0.75. The power consumption by the proposed circuit is also presented in this literature. The proposed design has been realized with QCADesigner version 2.0.3.

***Index Terms*—**Quantum-dot Cellular Automata (QCA), Fredkin Gate, QCADesigner, Energy dissipation.

I. Introduction

Due to the exponential diminution in element size in CMOS archetype, devices are further disposed to extreme leakage current and power dissipation. In accordance with Moore's law [1], every 18 months the measure of transistors that could be cohesive into a particular chip is doubled that causes in saving area and lessening device magnitudes. In this outlook, quantum-dot cellular automata (QCA) is the appropriate nominee that has not any of the mentioned complications and abilities particularly minimal power dissipation with small magnitude feature and high switching frequency [2]. Landauer [3] presented that, irrespective of the underlying technology, typical logic circuits deplete heat in an order of $kT\ln 2$ joules for every bit of information that is dropped. Afterward, Bennett [4] established that if computations are executed devoid of abolishing the information then rationally zero dissipation is possible. Because of favorable assets like minimal extent, extreme packing thicknesses and lower signal interruptions, QCA has achieved consideration in recent times. It was initially outlined in binary formula, however, multi-valued logic (MVL) which offers rapid implementation and inputs/outputs fall [5]. Besides, reversibility in a quantum computing is outlined a bijective relation concerning inputs to outputs that directs to minimize power dissipation. Rest of the literature is prepared as follows: Section 2 represents the synopsis of QCA and reversible logic. Section 3 signifies the proposed multi-layer Fredkin gate. The comprehensive comparison of the proposed gate with the existing designs are organized in Section 4. Overall power dissipation by the outlined circuit is discussed in Section 5. Lastly, conclusions are pointed in Section 6.

II. Summary: Background of Binary QCA

The binary quantum-dot is a four-sided cell alongside four quantum dots engaging the four apexes of the cell. Every single cell embraces two additional charges and the electrons can channel between dots and ultimately subjugate the antipodal locations due to Coulombic repulsion to complete minimal area [2]. Based on repulsion law of Coulomb, two electrons can individually engage antipodal positions in the cell. Therefore, each cell can encompass polarization status of either P = +1 or P = −1 with binary states 1 and 0, individually are explained in Figure 1.

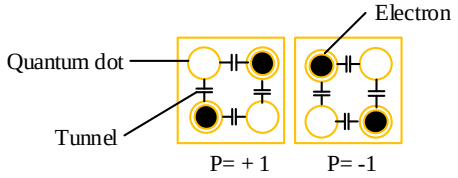

Fig.1. Four dotted QCA cell with binary encoding

The QCA assemblies of the essential gates are illustrated in Figure 2 to 4; specifically, QCA wire, majority voter and the inverter. QCA wires can be either made up of 45° cells or 90° cells. These cells used to transmit binary data from one side to another. Three input

majority voter (Maj_3) is the fundamental logic gate in QCA which can be comprised by five QCA cells where three used as inputs, one is output and another is the unique middle cell. The middle cell sometimes familiar as device cell that shifts to principal polarization [6] and determines the stable output. Quite a few designs based on basic building blocks of QCA are organized in [7-26]. The logical equation of Maj_3 is as follows:

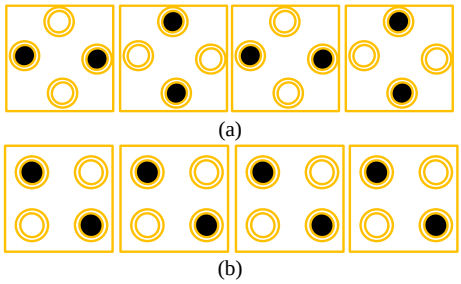

Fig.2. QCA wire (a) 45° (b) 90°

$$MV(A, B, C) = AB+BC+CA \quad (1)$$

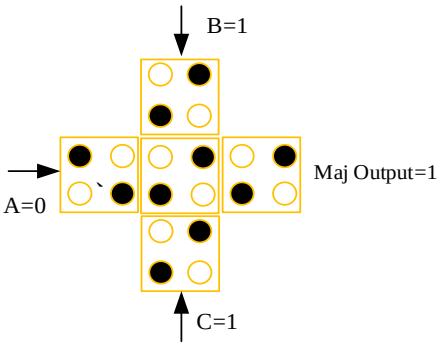

Fig.3. Fundamental form of 3-input majority voter gate

The QCA inverter basically transmits the cell polarization to the reverse polarization as presented in Figure 4. QCA circuits require apposite clocking to switch the flow of information that also supports essential power to operate the circuit. To operate the input to the anticipated output, signals need to be conceded through four stable clock zones [27] namely, Relax, Switch, Hold, and Release.

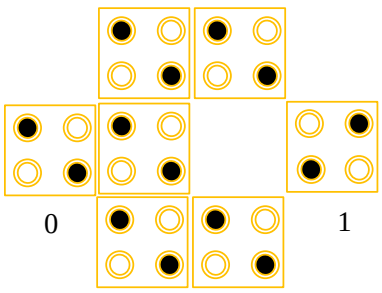

Fig.4. Seven cell QCA inverter

Clock signals for every single state are different and 90° phase shifted. The clocking flow is presented in Figure 5. Two particular kinds of crossover approach usually used in QCA circuit specifically, coplanar and multilayer. Multilayer crossover utilizes more than one layer of QCA cells, whereas coplanar crossover uses two separate cells for wire-crossing. In this study, multi-layer approaches are utilized [28].

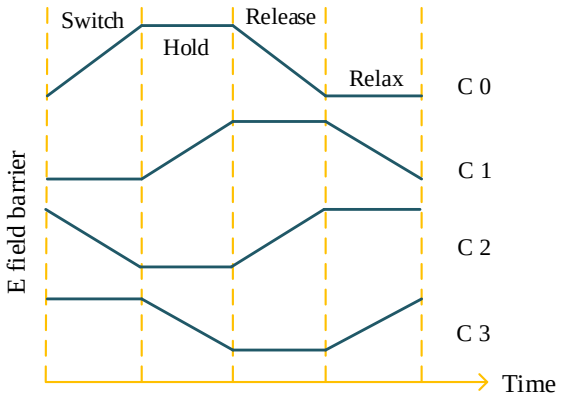

Fig.5. QCA signal for clocking zones

Reversible logic accomplishes the reversible purpose where the output shapes can be utilized to recuperate input outlines by reason of one to one mapping. Orthodox logic circuits cannot reinstate the inputs from the generated outputs, defined to as reversibility. In this phase, reversible computing in the field of nanotechnology, specifically, quantum computing, widespread studies have been considered. Two methodologies are there to realize reversibility: substantial reversibility and logical reversibility. Substantial reversibility indicates that there must be some requirements for computation in opposite manner. Logical reversibility defines bijective relation between outputs and inputs, thus inputs can be reasoned from the outputs. A number of efforts to implement reversible circuit have been completed in many scientific papers [10, 12-14, 18-23, 25, 26, 29]. Moreover, parity-conserving reversible circuits were designed in [30] for identifying inaccuracies in reversible circuits.

III. Proposed Fredkin Gate in QCA

Fredkin circuit is a 3×3 reversible logic circuit [31]. The stable input A, B and C to Fredkin circuit have distinctive output as P =AB+ A', Q = A'B+ AC and R = A. Its quantum charge is five [26]. The appropriate truth table is presented in Table 1 and majority voter-based equation of Fredkin circuit consistent to truth table as explained in Table 1 can be obtained as

Table 1. Truth Table of proposed Fredkin circuit

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

$$P = mv(mv(A, B, 0), mv(A', C, 0), 1) \quad (2)$$

$$Q = mv(mv(A', B, 0), mv(A, C, 0), 1) \quad (3)$$

$$R = A \quad (4)$$

The designed QCA structure of Fredkin circuit is presented in Figure 6 and QCA outline is in Figure 7. The proposed circuit is realized with only three majority voters and one inverter. Simulation result of designed gate is showed in Figure 8. Figure 8 establishes that for series of fixed inputs (A, B, C) as (0, 0, 0), the related series of outputs (P, Q, R) will be (0, 0, 0). For series of inputs (A, B, C) as (0, 0, 0), the relevant series of outputs (P, Q, R) will be (1, 0, 0). Correspondingly, for all input patterns, consistent results are presented in Figure 8. The results and the speculative values of Fredkin circuit as presented in Table 1 are equated which assesses the computation suitability of the proposed circuit.

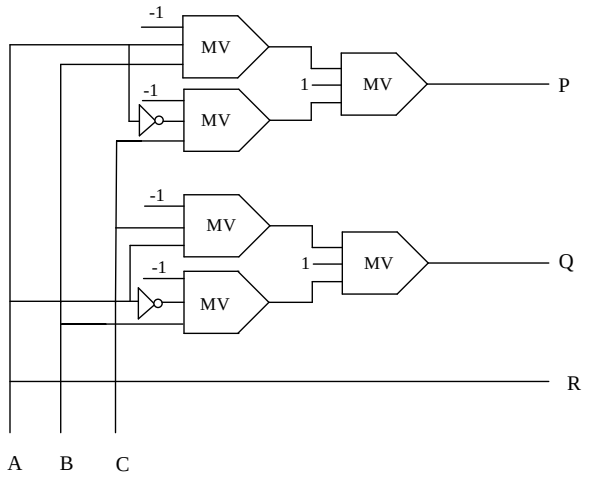

Fig.6. Proposed layout of Fredkin gate in QCA

The designed model has been functionally simulated with the QCADesigner ver. 2.0.3. Successive parameters in the bistable approximation and coherence vector simulation are employed which are the default forms in QCADesigner. These parameters are listed as: size of cell 18nm, temperature 1K, dot diameter, 5.0, samples number 12800, time step 1.0e-16, convergence tolerance 0.001, relaxation time 1.0e-15, radius of effect 65 nm, clock amplitude factor 2, relative permittivity 12.900000, layer separation 11.50, clock low 3.80e–023, clock high 9.80e–022, concentrated iterations per sample 100.

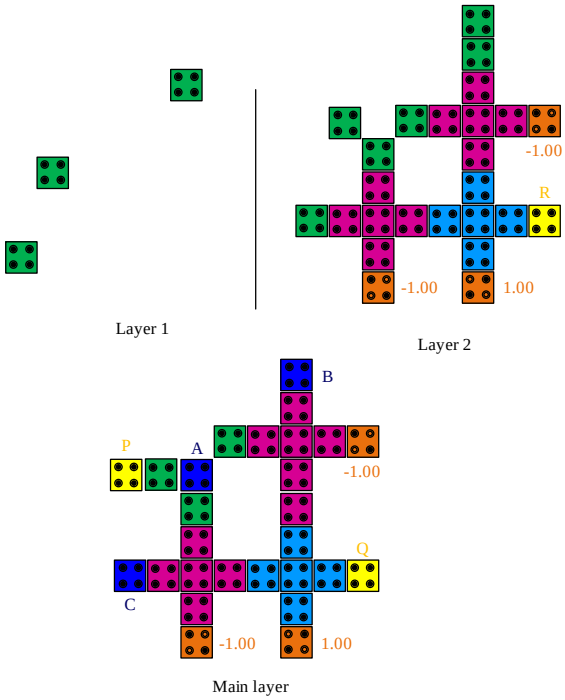

Fig.7. QCA simulated circuit design of proposed Fredkin gate

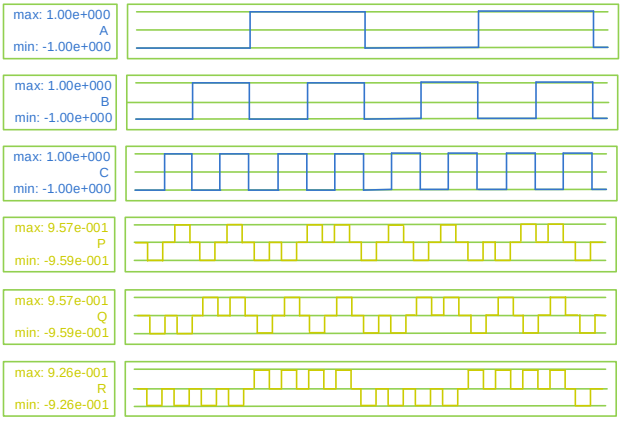

Fig.8. Simulated waveform for Fredkin gate

IV. Intricacy Study and Comparison Analysis of Proposed Fredkin Circuit

The hardware complications of the outlined design are organized in Table 2. From the table, it is perceived that the proposed Fredkin circuit requires three majority gate and single inverter. Number of cell required to design the gate is 55, and the area utilized by Fredkin gate is 0.03 μm^2. The cell extent of Fredkin gate is 0.018 μm^2 which outcomes in 60% area use regarding the overall extent.

The outlined QCA design of Fredkin circuit is compared with the existing designs [19, 32–37] as presented in Table 2. The outlined Fredkin circuit has 30.38, 28 and 57.14% enhancements over [19] in terms of figure of cell, cell area, and total area, correspondingly,

while over [36], the enhancements are 69.10, 68.97, 85 and 25%, in terms of overall cell, cell area, total area and latency respectively. Likewise, other enhancements are assessed and presented in Figure 9. The assessment evidently defines that the outlined circuit is faster and enhanced than that of the existing ones.

Table 2. Performance criterions of proposed circuit

Parameter	Proposed	Design in [19]	Design in [37]	Design in [36]	Design in [32, 34]	Design in [33]	Design in [35]
Cell intricacy	55	79	88	178	191	243	246
Cell area (μm^2)	0.018	0.025	0.028	0.058	0.061	0.078	0.080
Total area (μm^2)	0.03	0.07	0.098	0.2	0.22	0.34	0.37
Area usage (%)	60	35.71	28.58	29	27.72	22.94	21.62
Latency	0.75	0.75	0.75	1.0	1.0	1.0	1.0

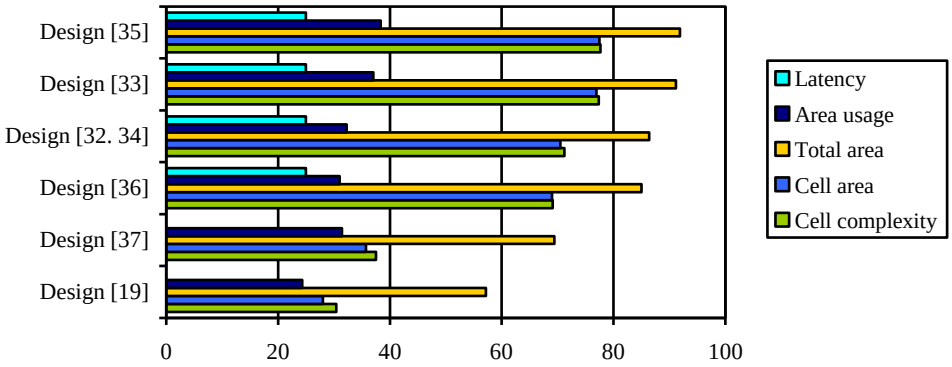

Fig.9. A reasonable study of proposed Fredkin gate

V. Power Dissipation by Proposed Circuit

Power dissipation assessment is a vital aspect in QCA circuit [38]. This part presents the overall power depletion by the designed circuit. The procedure organized in [39] is utilized to realize the depleted energy by the designed circuit in this study. The total depleted energy by any QCA circuit is deviated based on the utilized majority gate along with the number of used inverters [39].

Because of intrinsic nature, every single QCA cell in a circuit has consistent power depletion. Power consumption of QCA circuit will be elevated if the number of inverters and majority voter is raised. During a single clock cycle, the dissipated energy by any QCA layout can be estimated by accumulating the power consumption of all inverters as well as majority gates. Hamming distances between input variation to majority gate and to inverter are used to estimate their power dissipations [39]. The assessment is completed at several levels of channeling energy. The functional temperature is measured at T = 2 K. The estimation outcomes corresponding to Table 3 is surveyed in Figure 10. The symbolizations T, γ, E_k are utilized to characterize the temperature in which the procedure is carried out, channeling energy, and kink energy, correspondingly.

The competence of the proposed design under thermal unpredictability is verified in this study. To verify the proficiency, the polarization outcome on each output cell at several temperatures is perceived [40]. The results are presented in Figure 11 which clarifies that by growing the temperature, the average output polarization (AOP) for every single output of the proposed circuit is reduced.

Table 3. Power dissipation by proposed circuit at T=2 K

Design	Power depletion			
	γ =0.25 E_k	γ =0.50 E_k	γ =0.75 E_k	γ =1.0 E_k
Fredkin gate	98.3	101.8	107.3	113.6

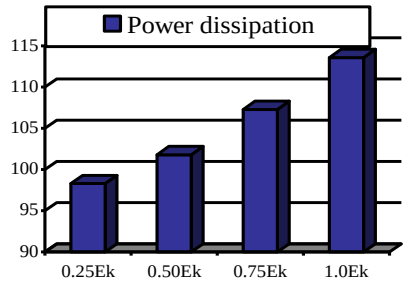

Fig.10. Power dissipation by the proposed Fredkin gate

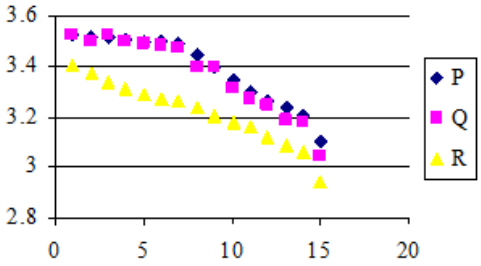

Fig.11. Temperature influence of the proposed circuit

The circuit executes competently up to temperature T = 14 K and after this temperature, the AOP of every output is very minimal, and the signals reduce. QCA Designer is utilized to attain AOP for every single output cell. For instance, the highest and lowest polarization for output cell 'Q' of proposed circuit is 9.57e–001 and -9.59e–001 at temperature T = 1 K, correspondingly. Therefore, the AOP for output cell 'OUT' is calculated as [(highest polarization+ lowest polarization)/2=] 3.524 as presented in Figure 11.

VI. Conclusion

In nanoscale logic design, device density and heat depletion are the perplexing concerns. QCA and reversible logic together can resolve these issues. In this literature, an efficient reversible Fredkin logic gate is proposed. We survey the performance of the proposed circuit and then compared with the existing layouts. The designed Fredkin circuit is faster and improved than that of the previous models and offered considerably enhancement overall measured metrics for example extent, cell extent, delay and complexity. Besides the power depletion and reliability of the proposed circuit is reported. Energy depletion by the proposed circuit indicates that the design depletes minimum energy. The assessment of simulation outcome with truth table defines the design precision of the circuit.

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