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Design of Low Power Sequential Circuit by using Adiabatic Techniques

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***Abstract*—** Various adiabatic logic circuits can be used for minimizing the power dissipation. To enhance the functionality and performance of circuit two adiabatic logic families PFAL and ECRL have been used and compared with CMOS logic circuit design. In this paper, A MASTER-SLAVE D flip-flop is proposed by the use of SPICE simulation on 90nm technology files. The simulation result shows that PFAL is a better energy saving techniques then ECRL logic circuit.

***Index Terms*—** Adiabatic Switching, Energy Dissipation, AC Power Supply, Inverter, D Latch and D Flip-Flop.

I. Introduction

The expression 'Adiabatic' is taken from a Greek language which means no energy transfer with outer environment, this process is known as a thermodynamic. So the dissipated heat loss in adiabatic logic families is very less. But in CMOS logic design, charge flow in the circuit is studied and many methods can be used for minimizing power dissipation in basic CMOS design like: reducing the power supply and switching activities. A combination of above all is important in portable systems which have some common issues such as weight, size and life of battery [2, 4, 27].

In today's modern era power dissipation is a primary concern in many application especially based on high performance battery operated and portable systems. By reducing the heat dissipation many digital signal-processing system can improve in performance of the systems.

The switching power and energy dissipation of static, completely restoring CMOS logic can be derived from the use of simple charge and energy conservation principle. Consider a CMOS logic design in Fig.1.

Here, if pull-down network is on and pull-up network is in cut-off region, the load capacitance (CL) at output is discharged through ground. Where if pull-down network is in cut-off region and the pull-up network is on then the current will flow from supply of power V_{DD} to the load CL until the output reaches V_{DD} [2, 13].

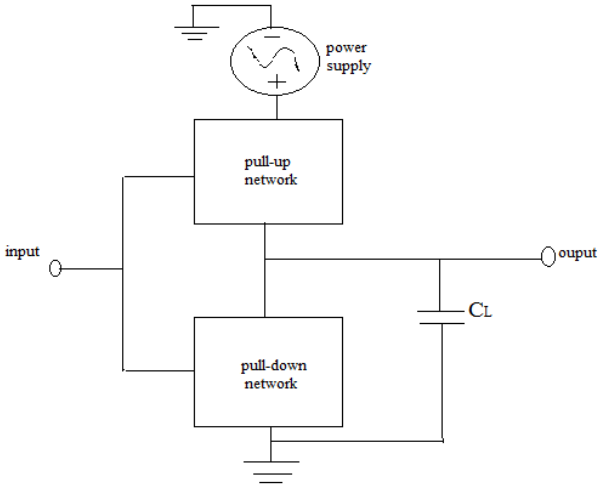

Fig. 1. Basic CMOS circuit design

In a charging process of output, a size of charge delivered to the load is [1].

$$Q = C_L.V_{DD} \quad (1)$$

Where, C_L is load capacitance and V_{DD} is the power supply. If the voltage is 0 then no energy is conveyed by current returning through ground terminal. A node V_{DD} charged up with energy is [1].

$$E = Q.V_{DD} = C_L.V_{DD}^2 \quad (2)$$

The half of power is stored in load capacitance $1/2C_LV_{DD}$ through V_{DD} and the rest of half power must be dissipated as heat by a PMOS resistor in pull up network. In conventional CMOS circuits the energy is dissipated at the time of the discharging process, which cannot be recovered [14].

The energy dissipation can be reduced by computation of adiabatic logic family during the charging and discharging process, and some of the energy is reused by recycling from the CL. [1, 2, 14].

Adiabatic logic families can be used to design low power memory components which further can be used in various applications [28].

Adiabatic logic works with the energy recovery principle where all charge transfer occurs without any heat dissipation. In adiabatic logic the charging and

discharging of load capacitance adiabatically is known as adiabatic switching [1, 2]. The adiabatic charging principle gives a way to charge load capacitor/parasitic capacitors via a resistor without dissipating $1/2C_LV_{DD}^2$ of energy [20]. As shown in Fig.2. The adiabatic logic circuits utilize AC supply voltage instead of the DC supply voltage.

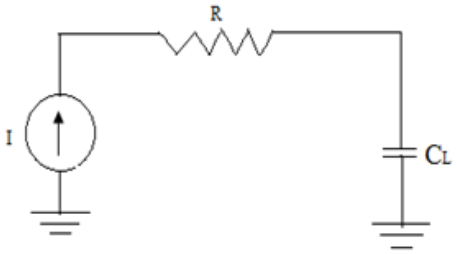

Fig. 2. Adiabatic logic design

In above circuit, the charge transferred is $Q = C_LV_{DD}$ and the average current will be $Q = C_LV_{DD}/2$ (Q is transferred charge to the load) so, the computed dissipated energy is [20].

$$E_{DISS} = I^2.R.T = \left(C_L.\frac{V_{DD}}{T}\right)^2 R.T = (2R.C/T).(1/2C_LV_{DD}^2) \quad (3)$$

Here, EDISS = dissipated energy due to the charging time,

C_L = load capacitance,

V_{DD} = power supply,

T = time of charging,

R_{ON} = ON resistance value of the PMOS,

The energy dissipation (EDISS) is highly depended uponR_{ON}, so the energy dissipation can be reduced by minimizing the R_{ON} of PMOS network. The first order approximation of R_{ON} is given as: [13, 20, 24].

$$R_{ON} = k(1/(V_{GS} - V_{TH})) \quad (4)$$

$$k = \mu C_{OX}\frac{W}{L}$$

Where, U= mobility,

C_{OX} = oxide capacitance,

W= width,

L= length,

V_{GS} = gate to source voltage,

V_{TH} = threshold voltage,

The result due to the "adiabatic principle" is a very slow change in systems which dissipate less energy than the fast ones; due to dissipation rates are proportional to the rate of change [20]. The equation (3) shows that it is also possible to minimize the energy dissipation by increasing the switching time values.

This is known as the adiabatic charging principle and the "adiabatic" term we are using here to indicate that all transferred charge is occurring without generating the heat [2]. The partially/quasi adiabatic ECRL and PFAL techniques have been implemented and discussed in this paper.

In this paper: In Section II, operation and basic concept of ECRL and PFAL Adiabatic Logic are discussed. In Section III, a D flip- flop is described by using D-LATCH. Simulation results of inverter and D flip-flop are shown in Section IV and Section V shows conclusion.

II. Operation of ECRL and PFAL Adiabatic Logic

Adiabatic logic circuits manifest their efficiency in real applications. In adiabatic logic there are four phases, evaluate/pre-charge, hold, recovery and wait. Adiabatic circuits deliver energy in pre-charge phase and then recover it in the evaluation phase [1-4]. In Fig.3 According to new method, the load capacitance gets charged (in evaluation phase) and discharged (in recovery phase) through a clock power by CMOS transmission gate, and controlled by inputs. ECRL works on both (pre-charge and evaluation) phase simultaneously. Hold phase maintains the values (low and high) and then use these values as input for evaluation to next stage [4].

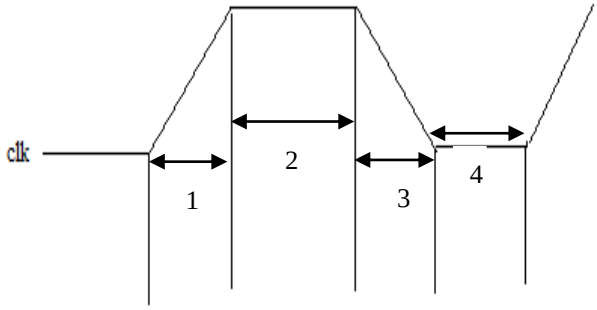

Fig. 3. Diagram of four phase logic for ECRL and PFAL

1. Pre-charge phase/evaluate phase
2. Hold phase
3. Recovery phase
4. Wait phase

A. Efficient Charge Adiabatic Logic

The proposed circuit of ECRL inverter gate uses the four phase clocking rule, the schematic and simulated waveform is shown in Fig.4 and Fig.5 simultaneously.

The 'evaluation/precharge phase' when input "a" is 1 and inverterd input "ab" is 0, the clk varies from 0 to vdd then the output "out" will be at ground level and "outb" will follow the pck (power clock).

As clk signal reaches to vdd, out and outb will enter into 'hold phase' (hold the logic value 0 and vdd respectively). Now after the hold phase clk signal goes from vdd to 0, the delivered value will recover and outb returns its energy to clk in 'recover phase'.

ECRL uses 4-phase clock rule to recover all charges delivered through the clk signal, the next stage should be in the evaluation phase, if previous stage is holding the valid phase [4, 14].

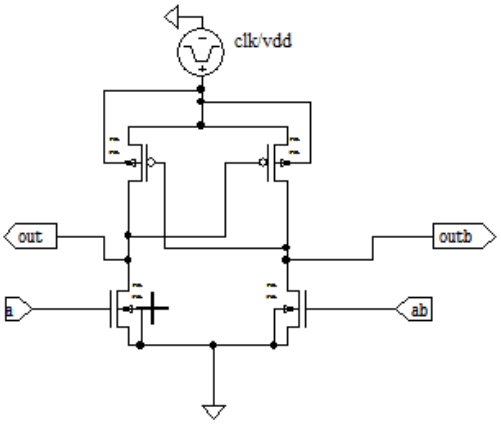

Fig. 4. ECRL logic inverter

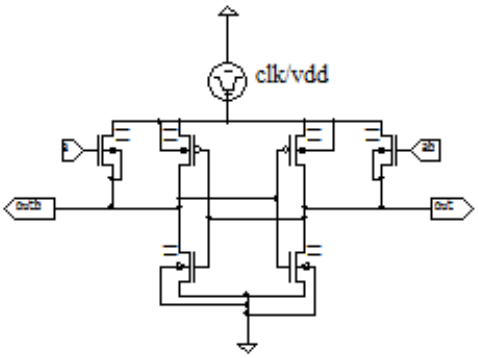

Fig. 6. PFAL logic inverter

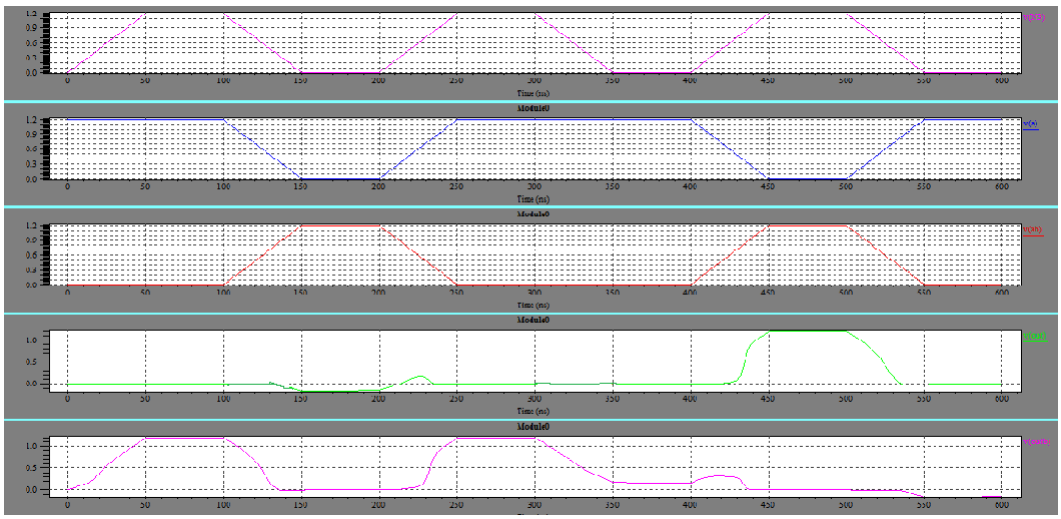

Fig. 5. ECRL and PFAL inverter waveform

B. Positive Feedback Adiabatic Logic

The proposed circuit of PFAL inverter gate is also utilizes the 4-phase clock rule, the schematic and simulated waveforms are shown in Fig.6 and Fig.5 simultaneously.

During ‘evaluation phase’ when input “a” is 1 and input bar “ab” is 0, the power clock “clk” goes from 0 to vdd then out will be at ground level and outb will follow the clk signal. As clk (Power Clock signal) reaches to vdd, out and outb will enter in ‘hold phase’ (hold the logic value 0 and vdd respectively).

Now after the hold phase clk signal goes from vdd to 0, the delivered will recover and outb returns its energy to clk ‘recover phase’.

Then ‘idle phase’ will be inserted to manage the symmetry of clock, the authentic inputs are being produced in the wait stage. In wait phase, right inputs arebeing prepared in last stage [5, 14].

III. D Flip-Flop Using D-Latch

In digital circuit design there are various applications made by D-LATCH for temporary storage of data or as a delay element. Consider a conventional CMOS D-LATCH in Fig.7 which shows a basic two-inverter loop and two CMOS transmission gate switches. Here, D is a single input. If ck is high then Q (output) will follow value of the input D and when ck goes to zero, the Q or the information will preserve its state as the inverter loop. Hence, the ck input acts as a signal which allows data to be latched into the circuit when ck=1.

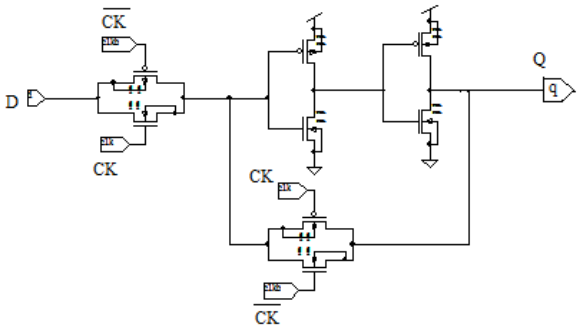

Fig. 7. CMOS D-LATCH

In Fig.7 this circuit is not an edge-triggered storage circuit because the final outcome depends on the input hence; the latch is transparent when ck is high. So this drawback makes it unsuitable for some applications like counters. For removing this drawback considers a two stage MASTER-SLAVE flip-flop circuit in Fig.8 which is designed by cascading two D-LATCH circuits.

The master stage is driven by ck signal and slave stage is driven by ck signal. So, the slave part is negative level-sensitive, while master part is positive level-sensitive.

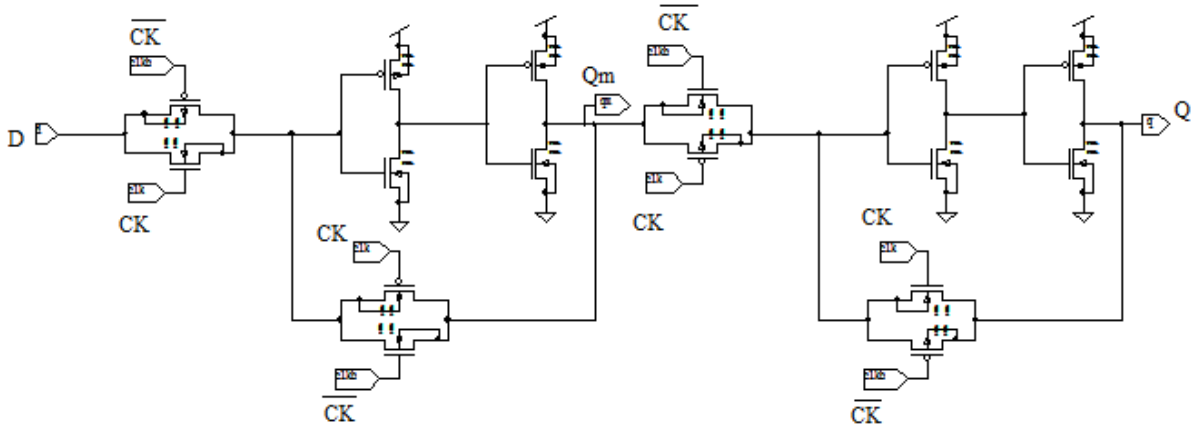

Fig. 8. Edge-Triggered master-slave D flip-flop

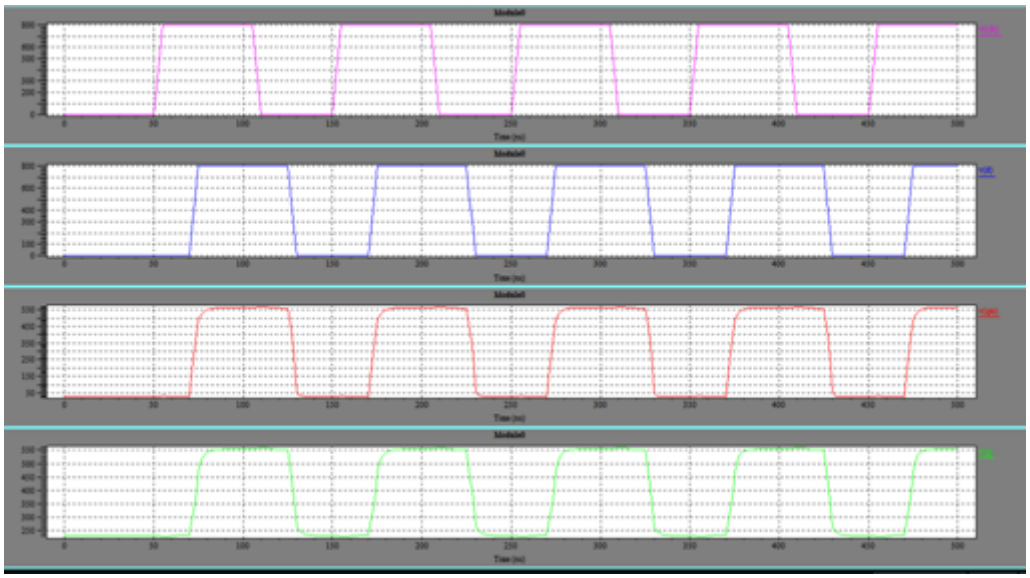

Fig. 9. simulated waveform of CMOS d flip-flop, ECRL and PFAL D flip-flop

IV. Simulation Results

The proposed sequential circuit D flip-flop is simulated by the use of SPICE tool based on 90nm technology. For this simulation we have used W/L ratio for NMOS transistors is 135nm/90nm and for PMOS transistors it is 405nm/90nm.

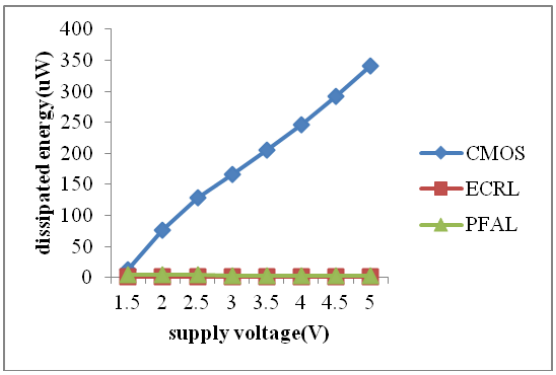

Fig. 10. supply voltage vs power dissipation for an inverter at frequency=10MHz on 90nm technology

The power consumed by the ECRL inverter and PFAL inverter at various voltage power supplies ranging from 1.5V to 5V is plotted in Fig.10.

ECRL D flip-flop and PFAL D flip-flop at various power supply variations form 0.9V to 1.2V is plotted in Fig.11. The result has been compared with conventional CMOS circuit design.

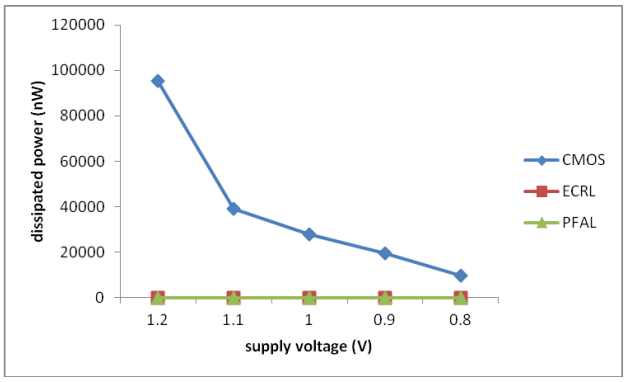

Fig. 11. supply voltage vs power dissipation for a D FLIP-FLOP on 90nm technology

Here, it can be seen that in Fig.10 and Fig.11 the gap in between adiabatic logic families and CMOS logic is reducing as supply voltage minimized.

Adiabatic logic families are strongly dependent on parameters variation [17]. Fig.12 and Fig.13 shows graphical representation of frequency versus dissipated power in traditional CMOS logic inverter and a sequential circuit D flip-flop at 1.5V and 1V power supply simultaneously.

For the comparison purpose the ECRL logic and PFAL logic is compared by CMOS logic design at frequency ranging from 0.1MHz to 1 kHz.

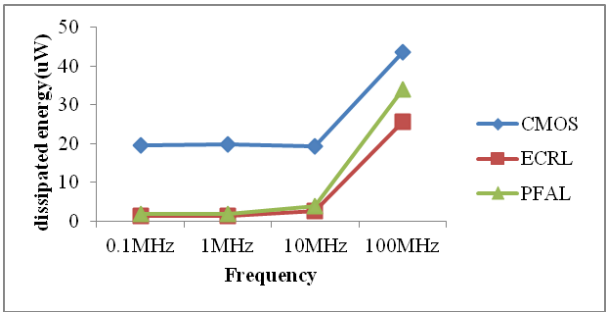

Fig. 12. Frequency vs power dissipation for an inverter at VDD=1.5V on 90nm technology

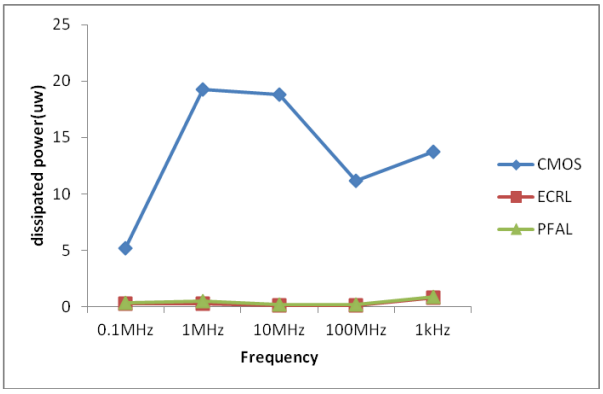

Fig. 13. Frequency vs power dissipation for a D FLIP-FLOP at VDD=1V on 90nm technology

Table 1. Summary of the results for Fig.10 and Fig.11

D FLIP-FLOP			
VDD (V)	CMOS (u WATT)	ECRL (u WATT)	PFAL (u WATT)
Frequency variation on Technology – 90nm at 1V			
0.1MHz	5.187044	0.31157	0.370773
1MHz	19.23786	0.311697	0.487944
10MHz	18.77796	0.157406	0.185722
100MHz	11.19761	0.157006	0.166279
1kHz	13.73116	0.79592	0.853199
Supply voltage variation on Technology – 90nm			
1.2	95530.18	0.132983	0.108913
1.1	39136.1	0.11151	0.089708
1	27715.08	0.092326	0.0756
0.9	19592.88	0.07461	0.06117
0.8	9678.32	0.059086	0.048556

Here, we can see that as frequency is increasing power dissipation is reducing and at very high frequency again it starts increase in power dissipation. Hence, it is investigated that at high frequencies, the behavior is no more adiabatic [13, 17].

But still PFAL and ECRL logic families consumes less power dissipation in circuit design by varying the parameters in circuit.

Adiabatic logic families show a advancement w.r.t CMOS, because of a high number of transistors needed in adiabatic implementation comparatively by the traditional CMOS implementation.

V. Conclusion

A D flip-flop circuit is designed with the help of inverter by using two adiabatic techniques ECRL, PFAL and a traditional CMOS have been successfully implemented to study the power consumption of digital and sequential circuits. The four phase clocking rule is used for to recover the efficient energy. The result has been carried out by using TSPICE simulation on 90nm technology files. It is investigated that PFAL and ECRL logic are even a better energy saving techniques as traditional CMOS. It is found that at high frequency the behavior is no more adiabatic. In overall conclusion, adiabatic logic can be used for low power circuits in VLSI design which reduced the energy dissipation over traditional CMOS logic design circuits.

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