I.J. Education and Management Engineering, 2013, 2, 35-39

Published Online February 2013 in MECS (http://www.mecs-press.net)

DOI: 10.5815/ijeme.2013.02.06



Available online at http://www.mecs-press.net/ijeme

Numerical Images Acquisition and Transmission Based on Microcontroller and CPLD

Minjin XIAO

School of Electronic Information & Electrical Engineering Changzhou Institute of Technology Changzhou,
China

Abstract

This paper presents a digital image acquisition and transmission methods. Using CMOS image sensors, under the control of the CPLD and microcontroller with a USB module, the system realizes the digital image acquisition and transmission. The design principle and system implementation are discussed in this paper. The system has high integration, small size and easy to install and portable .It can be well integrated with pre-processed data and image processing module, this will improve the efficiency of the computers operation. For digital image acquisition applications, size and power consumption are key considerations for hardware and software design problems, the CMOS image sensors used in digital image will have broad prospects.

Index Terms: Digital image acquisition; microcontroller; CPLD; USB transmission

© 2013 Published by MECS Publisher. Selection and/or peer review under responsibility of the International Conference on E-Business System and Education Technology

1. INTRODUCTION

CMOS image sensor is a new digital image sensor. As a result of CMOS technology, CMOS image sensors can support the pixel array and peripheral circuits (such as the image sensor core, single-clock, all the sequential logic, programmable functions and ADC) integrated in the same chip. Compared with CCD, CMOS image has advantages of high integration, small size, light weight, low power consumption programming convenience and easy to control. The system uses CMOS digital image sensor and MCU with USB module to realize the digital video image acquisition and transmission. This image capture and transmission mode has the advantage to achieve the digital acquisition and digital transmission. As CMOS image sensor with integrated ADC, the system does not require dedicated A/D converter. MCU has USB bus module itself. The system has high reliability and anti-jamming capability.

2. Hardware Composition and Working Principle

Image acquisition system consists of three major components: CMOS image output circuit, CPLD image

* Corresponding author. E-mail address: xiaomj@czu.cn control circuit and USB2.0 image data transfer. Figure 1 is the system block diagram.

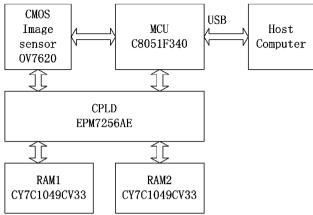


Fig 1. System block diagram

System chosen CMOS digital image sensor to direct the output digital image signal, so no need to use a special A / D converter to achieve digital video image signal. System consists of CMOS image sensors, with USB module MCU, CPLD and the memory component. MCU is the main control device, to achieve the control of CMOS digital image sensor, and transmit digital image signals to the host. System image sensors use OminiVision company OV7620 CMOS digital image sensor. OV7620 is an integrated a $640 \times 480 = 307 \ 200$ pixels (300,000 pixels) image matrix color camera chip, built-in 10 pairs of channel A / D converter, in the interlaced scan mode, the operating frequency up to 60Hz, by line scan is 30 frames / s. Image plane size is 1 / 3 inch. The chip supports 8-bit or 16-bit digital signal from the single-or dual-channel output. The output signal are of the type in YUV, YCrCb, and RGB. The image matrix supports VGA and QVGA image format. The digital output format are follow CCIR601, ZVPorts, CCIR656 standards. Video timing generator circuit can produce the synchronization, vertical synchronization, and other mixed-video synchronization signals and pixel clock synchronization and other timing signals. OV7620 has a strong camera and control functions, such as exposure control, y calibration, gain, color matrix, window choices, and can be programming control through the SCCB (serial camera controlbus) interface. ALTERA CPLD EPM7256AE is selected, the device has 256 macrocells, 16 logic array blocks and 164 maximum user I/O pins. In the system CPLD controls OV7620 lets the video data output into SRAM, and joint with the MCU to complete the video data USB transmission. The microcontroller use SILICON LABS C8051F430 MCU. It has full USB FLASH, built USB2.0 controller, support 8 endpoint integrated transceiver, 1KB of USB cache. It has a high-speed 8051MCU processing cores with the highest rate of 48MIPS and the maximum 4532B data RAM and 64KB FLASH memory. RAM selected Cypress CYTCl049CV33 static memory which has a 512KB storage space.

3. The Image Signal Acquisition and Transmission

A. Image Data Acquisition and Storage

0V7620 integrates a SCCB (serial camera controlbus) control interface, which support for SCCB set mode and automatically load the default settings mode, the choice of control by the SCCB. The system only needs to support SCCB mode. SCCB bus has the timing similar to the I2C bus timing, SIO-0 equivalent to SDA, SIO-1 equal to SCL. After power MCU set the OV7620 through the bus of SCCB. In the design, OV7620 work in slave mode, the process of writing the register sends the OV7620 ID address, and then send the purpose of writing the data register address, and finally send the data to be written. MCU working in the fast I2C bus mode. After power, single chip through I2C bus to read and write OV7620 chip register, set the sensor operating

parameters. After receiving the command of start acquisition from the host, the MCU will send image acquisition control signal to the image sensor. The sensor FREX, EXPSTB pin are all set to high. For some time after the EXPSTB pin set low, the image sensor began to frame exposure until the shutter closed, and the digital image signals are output. After frame exposure digital image sensors lets the data output in accordancewith its data synchronization signal. Through the CPLD control interface circuit, the digital image data are divided into two fields which are each sent to two independent SRAM. The CPLD has a memory control module, read control module and the memory switch module in the design. The control logic module of the CPLD is written by VHDL language, and is download to the chip after simulation with the design tool of QUARTUSII. 0V7620 provide data synchronization signal (pixel clock PCLK, field sync VSYNC, line synchronization CHSYNC, line reference HREF) and generate RAM write address and write enable signal for image data storage. CPLD read out control module counts the PCLK signal until the counter is full with 480K datas, CPLD produce memory switching signal SWITCHRAM. In order to achieve continuous acquisition of image data ,the CPLD uses the read data signals from MCU TTCOM interface to produce RAM read address and read enable signal. In the process of image data storage, CPLD storage control module send the image data to RAMI, when PCLK over 480K in mind, the memory switching module produced signal SWITCHR AM, the storage control module switch to the RAM2 to stores image data continuously, while the read out control module to the RAMI, then an interrupt signal is send to the microcontroller TTINT. Figure 2. is the CPLD interface map.

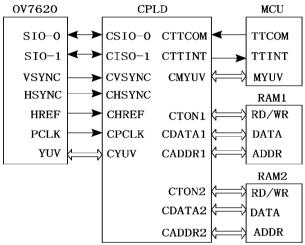


Figure 2. the CPLD interface map

CPLD work is set in the mode on the falling edge of PCLK signal to update data. In the rising edge of PCLK the data is stable .SRAM address signal ADDR are updated during the falling edge of the PCLK signal . The PCLK signal rising edge makes /WR signal effective, and then the data are writen to the SRAM.

B. Image Data Transmission

Image data transmission is start when the CPLD sends a interrupt signal . After the microcontroller receives CPLD interrupt, CPU enabled USB transceiver and send read data signals. USB function controller contains eight endpoints pipeline, in the design, the control endpoint (endpoint 0) is always a two-way IN/OUT endpoint, endpoint 1 configured as OUT endpoint pipes, endpoint 2,3,4,5 endpoint is configured to IN pipeline . The SPEED selection bit of Special Function Register USB0XCN is selected to make communication speed USB0 working in full speed mode. To send data, SIE interrupts the processor after finished sending a complete packet and received the corresponding handshake signal and through the CPLD control module, reads out the image data in the RAM in accordance with the endpoint data buffer address to microcontroller USBFIFO.

When the buffer is full, the MCU gives the contro of buffer to the USBSIE, and then CPU continues reading the next input data to the endpoint buffer. The host user program calls the Windows API functionand, sends input commands by useing USB driver and receives image data to achieve the continuous transmission of image data.

4. Software Design

The software design includes three parts, MCU program and USB device firmware, device drivers and applications.

A. MCU and USB Device Firmware

MCU program includes image sensors initialization procedures, USB module initialization procedures and the main program. Figure 3. is the MCU program.

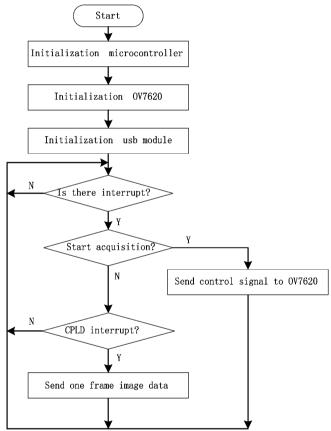


Figure 3. the MCU program

In the image sensor initialization procedure, the chip is set in the slave mode. The chip operating modes and camera video chips imaging parameters such as the size of the window are also set in the procedure. The USB module initialization procedure set the size and number of data buffers. In the design, the USB transfer type is the full-speed bulk transfer mode. Consider the data buffer size, the design enables the endpoint 0 (input, output), Endpoint 1 (output), Endpoint 2 (input), Endpoint 3 (input), Endpoint 4 (input), Endpoint 5 (input).

Procedures sets the USBRAM data buffer controlled by the microcontroller CPU and according to the selected data buffer set registers, including: USB Interrupt Enable Register, USB control, configuration, status registers, the endpoint registers and sets MCU interrupt levels and trigger conditions. The main program includes microcontroller I2C interface control software for OV7620 and CPLD handshake procedures. All procedures are carried out with the Keil C and download to the MCU.

USB device firmware programming in this design is to initialize the microcontroller and peripherals, sent USB request and in response to the host of standard equipment request and completing data transfer depending on the device functions. Initialization program sets the system clock, I/O port settings, and cross-switch settings, USB controller and the endpoint initialization. When the host is connected to the USB interface, it calls the driver with the host software and lets image data transmission to the host via USB interface .

B. Device Drivers

In the design, USB device driver uses standard WDM device drivers procedure. WDM uses IRPdriven mechanism. When the application I/O request is submitted, WDM calls the function WIN32API and sends an order to the equipment, then the I/O manager forms a IRP. After receipt of the IRP which gives the control codes, USB device driver finds the corresponding program entry.

C. Applications

In the application, the API functions are added to the corresponding functional module, then the operation of application can be completed for the USB device to open, read and write, so that the communication between the USB device and the application can be fully realized. Applications achieves the image display with the VGA or CIF image format. In the design the user interface uses VB and the data transmission is completed by calling for Windows API function. User program working process is as follows: the programm issues start collecting command to the device through the USB bus. After receipts of the memory full marks the programm gives a command of upload data to start the mass data transmission . The received image datas are displayed with VB real time image control.

5. Conclusions

The design presents a design and implementation of a digital image acquisition and transmission system, focusing on the working principle of the system hardware and functions of the software. Design innovation is the application of MCU and CPLD on CMOS image sensor control and signal processing, and achieves a digital image transmission through USB interface. The system has the characteristics of intelligence and high reliability and has broad application prospects in the field of industrial visual inspection .

References

- [1] Lizhaoqing, Liaofeng and Liujiancun. USB Interface technology. [M]. Beijing: National Defence Industry Press, 2004.
- [2] Mawei. Computer USB system theory and master/slave design.[M]. Beijing: Beijing University of Aeronautics and Astronautics Press, 2004.
- [3] Houshuzhi, Yaosuying and Zhoujin. CMOS Image sensor timing control method researches and implementation. [J]. Solid State Electronics Research and Development.vol.27,pp.119-122, February. 2007
- [4] OmniVision, OV7640 Data Sheet Version1.7, 2003.10
- [5] OmniVision, Serial Camera Control Bus (SCCB) Functional Specification, Version2.1, 2003.2
- [6] Siliconlabs.C8051f34x datasheet [EB/OL]. http://www.silabs.com. Revision0.5
- [7] MAX7000A Programmable Logic Device data sheet .[EB/OL]. http://www.altera.com.