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Comparative Analysis of Various SRAM Cells with Low Power, High Read Stability and Low Area

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Abstract

SRAMs are very important part of today's movable devices like laptops and mobile phones. Different SRAM cells of different number of transistors have their own respective advantages and drawbacks. In this work an attempt has been made to reduce the leakage power by adding some transistors. Each SRAM cell provides an efficient way to reduce the leakage power, but disadvantage of each SRAM cell limit the application of them.

In this paper, the study and transient analysis on four different SRAM cells has been carried out and compared with respect to various parameters like power dissipation, delay and area. The simulation is carried out in 180nm CMOS technology using tanner tools. Layout is carried out using microwind.

Index Terms: Delay, SRAM cell, SNM, Power Dissipation.

1. Introduction

The main objective of this work is evaluating performance in terms of power consumption, delay and area of various four SRAM cells in 180nm technology and comparing them with basic 6t SRAM cell.

Literature review and study of various SRAM cells is done. Transient analysis of all the SRAM cells is done and output is shown. The layouts are also shown. Result (power, delay and area) of all the SRAM cells has been shown and discussed. The project is developed in tanner tool v14.1. Microwind 3.1 is used for generating layout and calculating area.

Low leakage 10T SRAM cell has separated read port and stacked effect by M10 transistor, so it has BL leakage reduction feature [2].

High read stability 9T SRAM cell has separated read port so it has features of Read stability enhancement, 22.9% leakage power reduction and double read SNM as compare to 6T SRAM cell [3].

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Low write power 7T SRAM cell has 49% write power saving but it is 17.5% larger than 6T SRAM cell due to one extra transistor [4].

Single ended 5T SRAM cell has 75% BL leakage reduction, 50% lower SNM and 23% smaller area as compared to 6T SRAM cell [5].

1.1. Subthreshold 10T SRAM cell

As shown in the figure 1, it has separated read port i.e. separate BL and WL for read operation. Also it has stacked effect by M10 with M7 so the BL leakage is reduced.

To deeply understand the write operation, let us assume that WL signal is ON. So the pass transistor M2 and M5 connects the SRAM with signals BL and BLB. Now let us assume that, we have to write '1' at Q. So indirectly we are writing '0' at QB. For writing '1' at Q, we have to give '1' at BL and '0' at BLB. As the transistor M2 is ON because WL is high, so the data at BL directly forces Q to high and this is turn M4 ON and M6 OFF. So QB is discharged through M4 and becomes low, which alternately forces Q to high. So, finally we have logic 1 at Q.

To perform Read operation, we have to give logic '1' at WL so transistors M2 and M5 are turned on and also we have to give logic '1' at BL and BLB to read the value of Q at BL. The circuit with extra four transistors and two extra inputs RBL and RWL is used to reduce the leakage current of the SRAM cell. When we are performing read operation, we have to give logic '1' at RBL and RWL so transistors M8 and M10 are turned on and QB is inverted and output is stored at QBB, which is connected to RBL so we get the output at RBL.

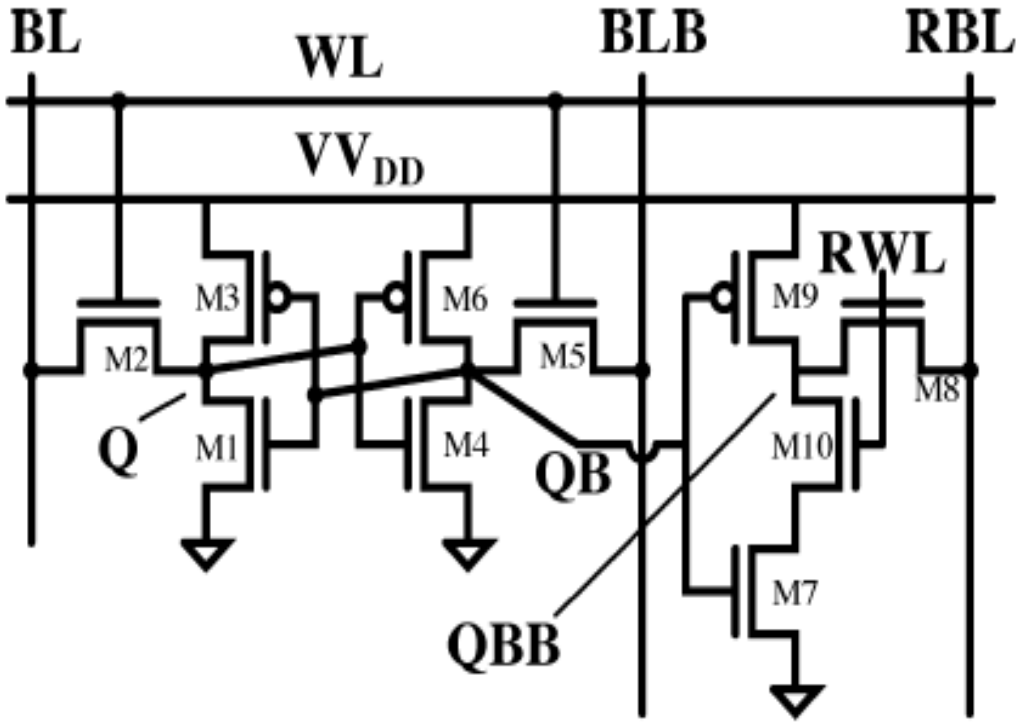

Fig.1. Sub threshold 10T SRAM cell

1.2. High read stability and low leakage 9T SRAM cell

As shown in the figure 2, it has three extra transistors and one extra input RD as compare to basic 6T SRAM cell. It has separated read port.

During write operation WR goes "high" and RD goes "low", so transistor N7 is cut off and transistors N3 and N4 are turned on. As we pull WR to 1, transistors N3 and N4 are turned on and what we give at BL is written to Q.

During read operation RD goes "high" and WR goes "low", so transistor N7 turned on. To read, we apply logic 1 at BL and BLB. If Q has Logic 1 then it turns ON transistor N5, so BL signal is discharged through N5 and N7 i.e. the value at Q is stored at BLB.

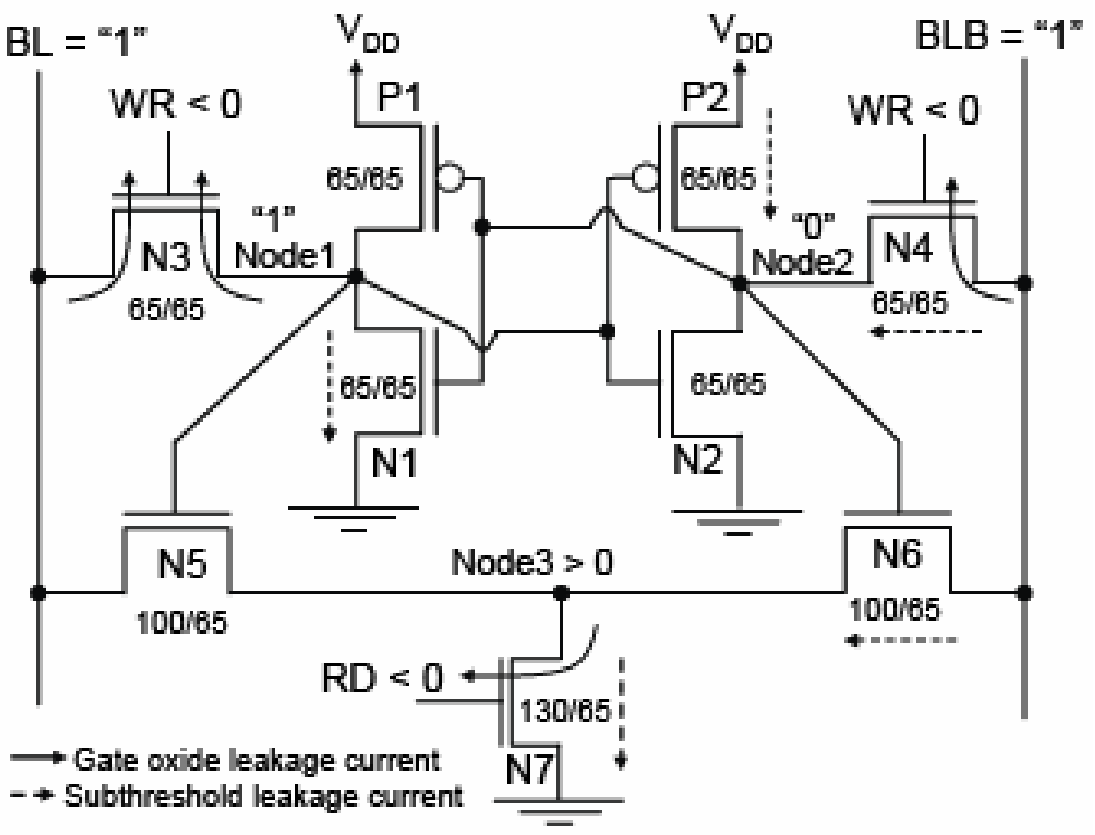

Fig.2. High read stability and low leakage 9T SRAM cell

1.3. Low write power 7T SRAM cell

As shown in figure, it has one extra transistor N5 and one extra input W as compare to basic 6T SRAM cell.

The write operation starts by turning N5 off to cut off the feedback connection by giving logic 0 at W. N3 is turned on by applying logic 1 at WL. N4 is kept off so BL is disconnected to the circuit. So finally the value given to BLB is directly saved at QB and inverted data of QB is stored at Q.

During read operation, it behaves like a conventional 6T SRAM cell i.e. N5 is kept on, which make it same as conventional 6T SRAM cell. When logic 1 is given to BL and BLB, the data at Q and QB charges or discharges BL and BLB accordingly. During all the process WL and R are given logic 1 so transistors N3 and N4 are turned ON to enable the read operation.

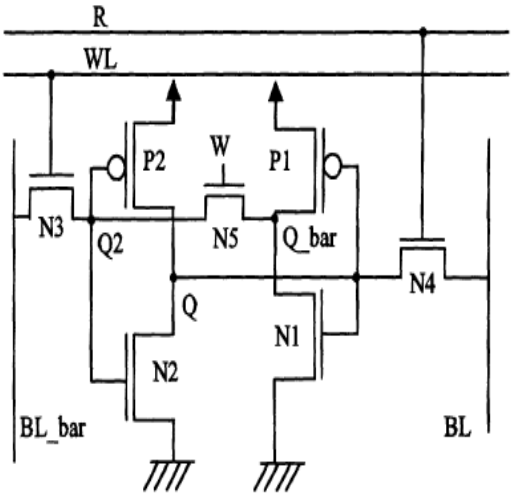

Fig.3. Low write power 7T SRAM cell

1.4. Single ended, low leakage 5T SRAM cell

As show in figure, it has single BL and single WL.
During read operation, BL is precharged to 600mV and then WL goes “high”, so the data at Q stored at BL.
During write operation, the data at BL is stored in Q as WL turns transistor M5 on.

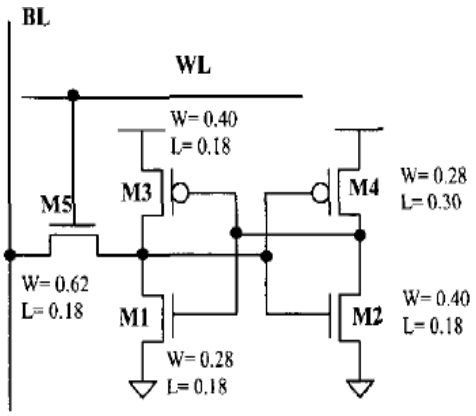

Fig.4. Single ended, low leakage 5T SRAM cell

2. Results and Waveforms

2.1. Subthreshold 10T SRAM cell

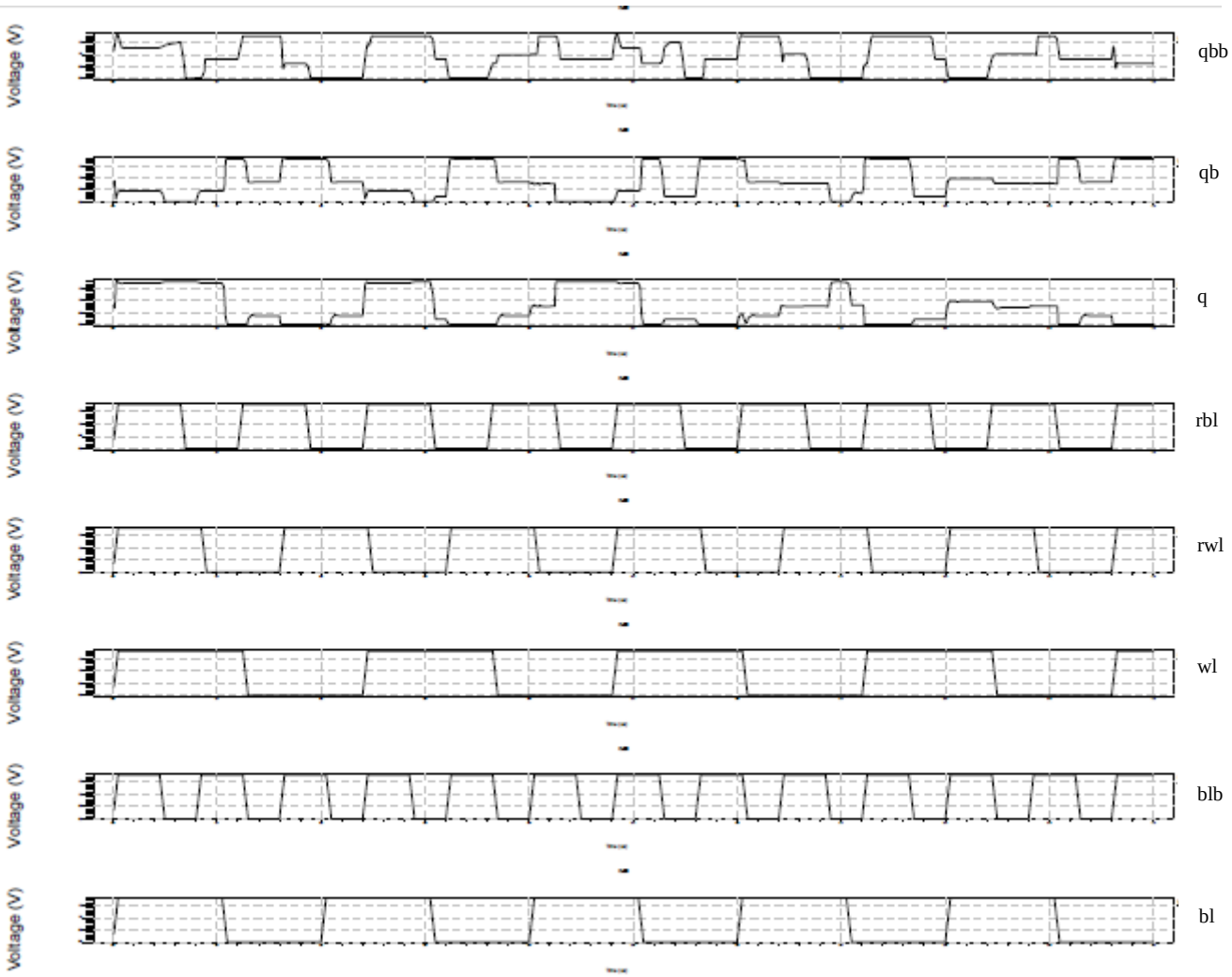

Fig.5. Output Waveform of Subthreshold 10T SRAM cell.

The subthreshold 10T SRAM cell has five inputs RBL, RWL, WL, BLB, BL and three outputs Q, QB, QBB as shown in waveform above. When WL is at logic '1', read or write operation takes place. When BL and BLB both are at logic '1', read operation is done i.e. the data at Q is taken at BL. When BL and BLB are different then each other, write operation is done i.e. the value of BL is written to Q.

Average power consumption is 9.175496 e-005 watts.

Read delay is 1.0950e-007 sec.

Write delay is 8.0360e-008 sec.

The layout shows that total area is 24.9*7.1 (um) ².

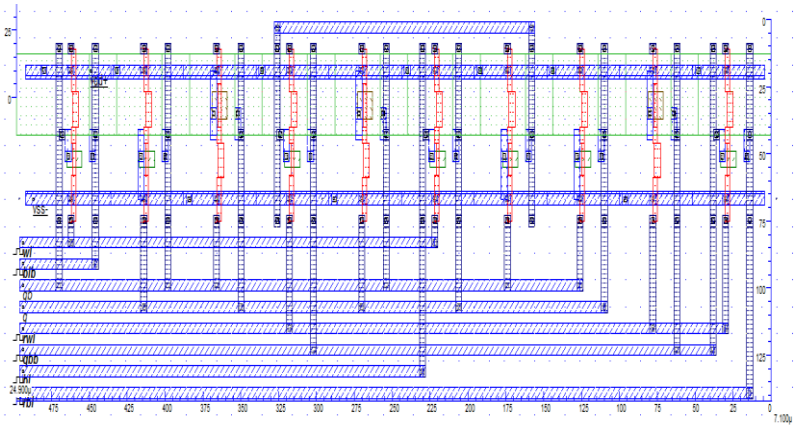

Fig.6. Layout of Subthreshold 10T SRAM cell

2.2. High read stability and low leakage 9T SRAM cell

Fig.7. Output waveform of High read stability and low leakage 9T SRAM cell

The high read stability and low leakage 9T SRAM cell has four inputs BL, BLB, WR, RD and two inputs Q, QB as shown in the waveform above.

Average power consumption is 1.092888e-004 watts.

Read delay is 6.5000e-008 sec.

Write delay is 2.0482e-009 sec.

The layout shows that total area is 22.5*6.2 (um) ²

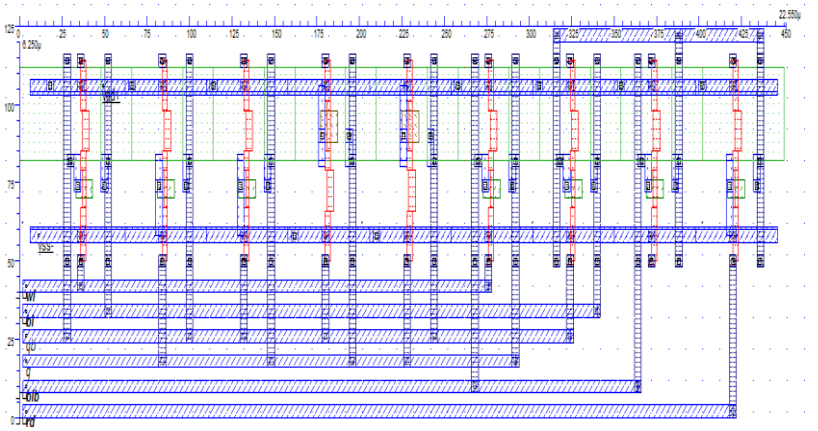

Fig.8. Layout of High read stability and low leakage 9T SRAM cell

2.3. Low write power 7T SRAM cell

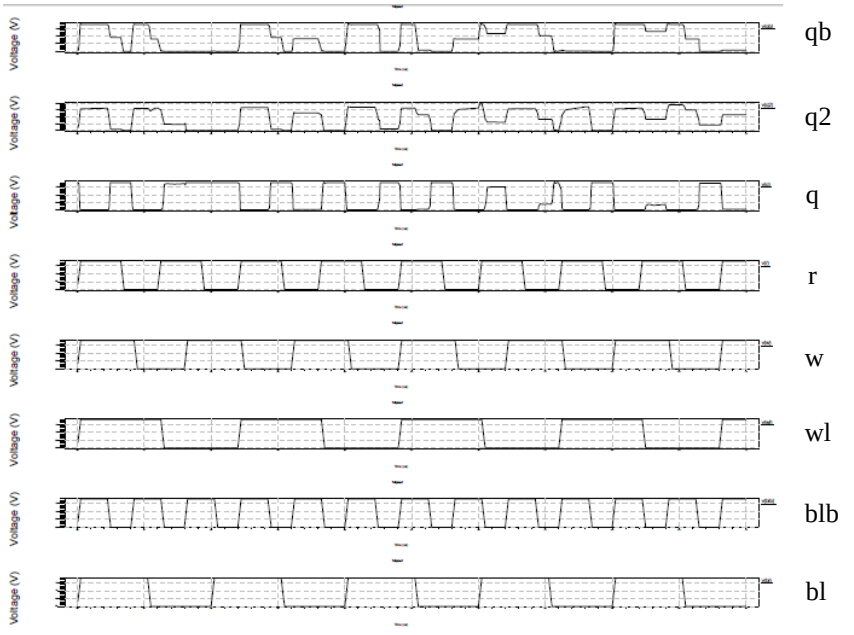

Fig.9. Output waveform of Low write power 7T SRAM cell

As shown in the waveform above, the low write power 7T SRAM cell has five inputs BL, BLB, WL, W, R and three outputs Q, Q2, QB which are measured and shown above.

Average power consumption is 2.358070e-005 watts.

Read delay is 1.275e-007 sec.

Write delay is 2.1e-007 sec.

The layout shows that total area is 17.7*6.6 (um) ².

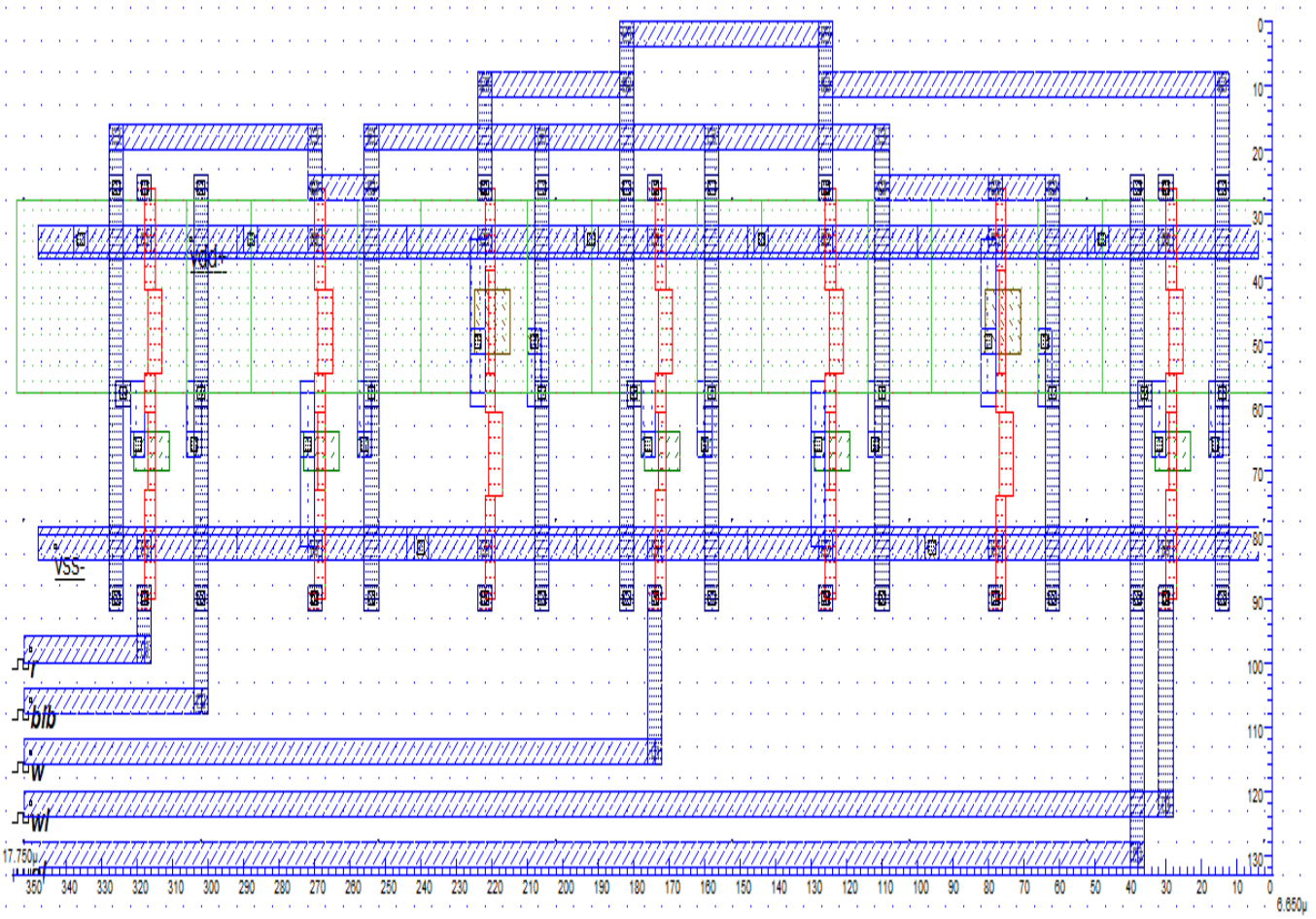

Fig.10. Layout of Low write power 7T SRAM cell

2.4. Single ended, low leakage 5T SRAM cell

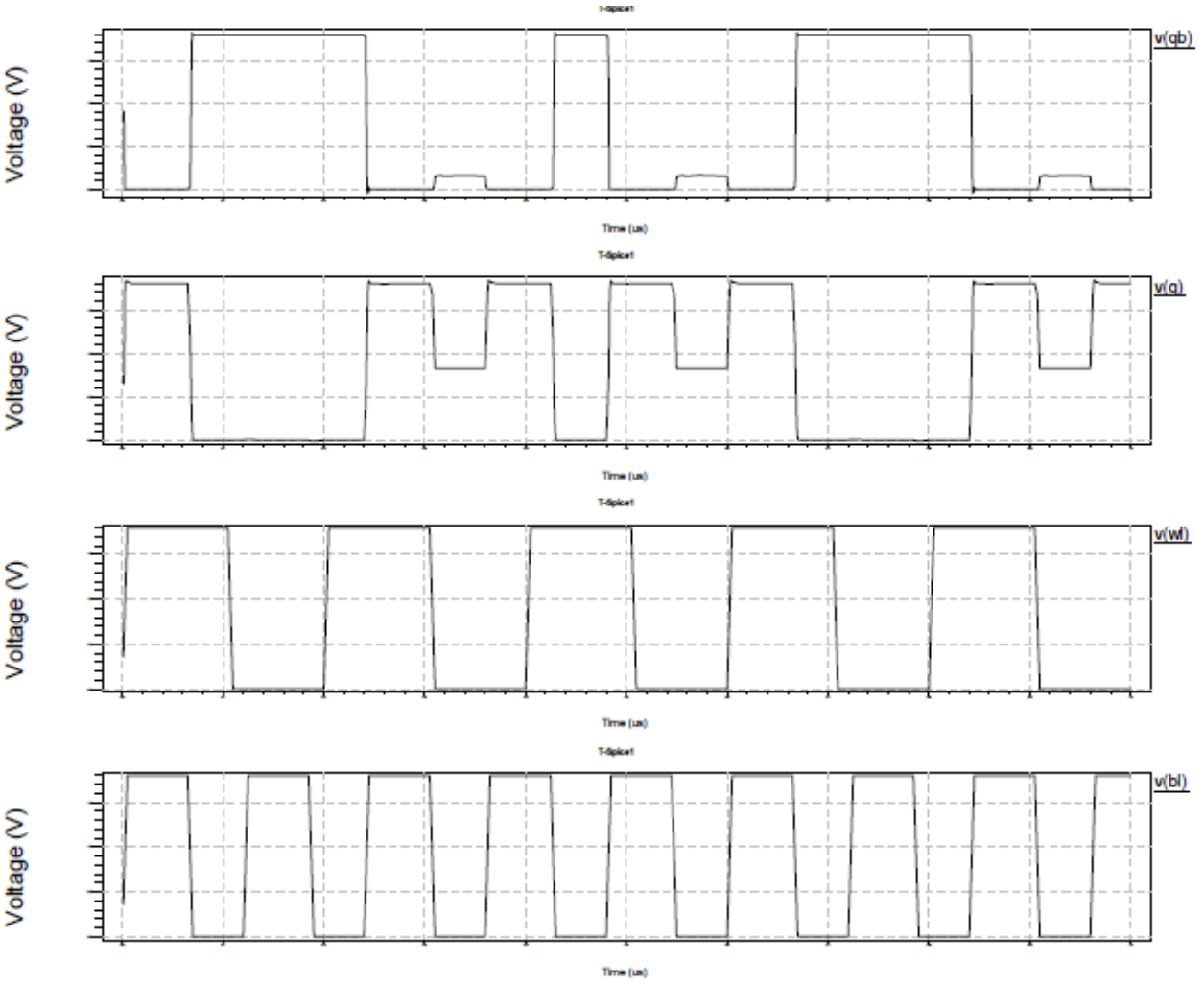

Fig.11. Output waveform Single ended, low leakage 5T SRAM cell

As shown above, this SRAM cell has two inputs BL, WL and two outputs Q, QB which are measured as above.

Average power consumption is 3.604690e-006 watts.

Read delay is 6.5000e-008 sec.

Write delay is 1.3064e-009 sec.

The layout shows that total area is 12.9*5.0 (um) ²

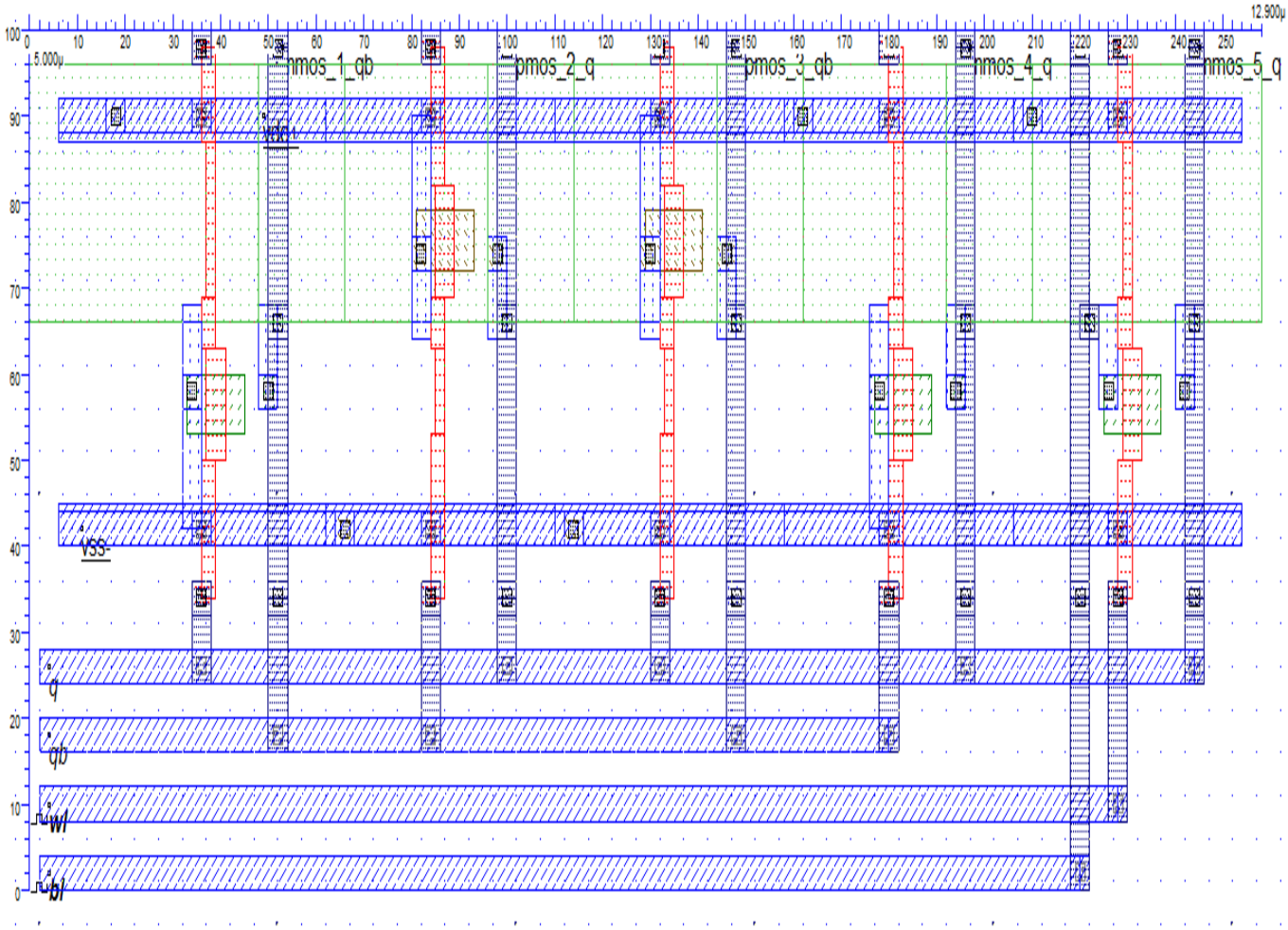

Fig.12. Layout of Single ended, low leakage 5T SRAM cell

3. Conclusion

Comparison of these four SRAM cells is shown in the table bellow according to the parameters power consumption, read delay, write delay, area.

Table 1: comparison of various SRAM cells

SRAM cell	*POWER CONSUMTION (uW)*	*READ DELAY (n sec.)*	*WRITE DELAY (n sec.)*	*AREA (um) ²*
Basic 6T	131.7	0.47	0.96	116.82
5T	3.6	65.0	1.3	64.5
7T	23.6	127.5	210	116.82
9T	109.3	65.0	2.0	139.5
10T	91.7	109.5	80.4	176.79

In this paper comparison of various SRAM cells is done with respect to parameters like power dissipation, read delay, write delay and area as shown in the table above by using tanner tools software. In these SRAM cells, the read, write delays and area are increased but power dissipation is much reduced accordingly. Even 5T SRAM cell has low area consumption with respect to conventional 6T SRAM cell.

Acknowledgements

For power constrained projects like space exploration and satellites the SRAM cell which consumes minimum power should be used while for very fast processing devices the SRAM cell which has minimum time delay should be used. The design of SRAM cell can be optimized by tradeoffs between various performance parameters.

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Author(s) Profile

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