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Analysis of Resistance Parasitic of Single Wall CNT bundle with Copper for VLSI Interconnect

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Abstract

The rapid technology advancement in VLSI leads to decreased in chip size to few nanometers. With such continues miniaturization of VLSI devices has strong impact on the VLSI technology in certain ways such as increase in resistance. The performances of ICs have been decreasing aggressively with increase in resistance, which furtherlead to increase interconnect delay thus becoming much more significant factor of problem. Thus traditional Copper interconnects have now become a significant performance delimiter due to increase in its resistance at Nano level. Thus to overcome from the limitation of Copper, Carbon Nanotubes have been proposed as a possible future replacement of Copper interconnect. Several different configuration of CNT proposed, out of which Single Wall CNT configuration has been received much attention for their unique characteristics and as a possible alternative to Cu interconnects in future ICs. In this paper we have compare the equivalent circuit model of Single wall CNTs against traditional Cu interconnectfor resistance parameter. For the first time an impact of length, width and mean free path on interconnect resistance is study at 22nm proving a CNT as strong replacement to Copper interconnect.

Index Terms: Interconnect, Copper (Cu), Carbon Nanotube, Single wall Carbon Nanotube (SWCNT), Multi Wall Carbon Nanotube (MWCNT), Mean free path (MFP).

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1. Introduction

With Development of ICs into nanometre scale leads to new challenges for copper. The major challenge mainly arises from the steep increase of copper resistivity which is due to surface scattering and grain boundary scattering. The reliability issue due to electromigration, heat dissipation, and the current capacity issue is also affecting the performance. The increase of resistivity in the IC interconnects could result in signal integrity issue, such as long time delay. This steep rise in parasitic resistance of copper interconnects poses serious challenges for interconnect delay especially at the global level where wires traverse long distances and

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for interconnect reliability, hence it has a significant impact on the performance and reliability of VLSI circuits.

However to run-over from such problems, change in the traditional used material for on-chip interconnections have been searched out and the most promising alternative for traditional copper interconnects turns out to be Carbon Nanotube (CNT). The CNTs are grown in the form of seamless cylinders with the walls formed by one atomic layer of graphite (graphene). The diameters of these cylinders are of the order of a nanometer. These tubes are either metallic or semiconductor. For interconnect applications the metallic ones are most suited and useful. There are two configuration of CNTs. Single walled CNT (SWCNT) and Multiwall CNT (MWCNT). CNTs having only one thin wall of graphene sheet are SWCNTs. There are some CNTs which consist of a multiple of concentric SWCNT like graphene tubes. These are termed MWCNT. The metallic CNTs are attractive for interconnect materials because of their high thermal and mechanical stability, thermal conductivity as high as 5800W/mK, ability to carry current in excess of 1014A/m2 current density even at temperatures higher than 200 ℃ and Fermi velocity comparable with that of a metal (DavoodFathi et al.,2010). It is very difficult to make a good contact with a CNT. The unavoidable contact imperfection increases resistance. CNT resistances in the range 7 KΩ - 100 KΩ have been reported. Such a high resistance is a major disadvantage; if an isolated CNT is used as interconnect. Thus to overcome from this problem and made it circumvented for interconnect application CNT bundles are used instead of isolated ones.

A CNT bundle consists of a large number of electrically parallel isolated CNTs. The result of the parallel connection is considerable reduction of resistance between the ends of the bundle. Therefore, a CNT bundle makes a better interconnect than the isolated counterparts. The type of CNTs in a bundle is generally either SWCNT, MWCNT or Mixed CNT (Mixed SW/MW CNT).

This paper work is aimed to do comprehensive analysis of the performance of Single Wall CNT bundle as VLSI interconnects vis-à-vis copper interconnects in a detailed manner. This analysis is used to identify the resistive parameter of SWCNT bundle interconnects that can be exploited to derive maximum benefit from them as well as that give rise to major limitations in their applicability as interconnects.

2. Interconnect Challenges At Nanoscale

The continued scaling of semiconductor devices from µm to nm in VLSI integrated circuits means that there is a replacement of the traditional materials. As, in the past we have seen that the aluminum wires are replaced with copper wires due to lower resistance characteristics, now copper wires are going through the similar problems due to the increasing resistivity and as a result, wire delay is becoming serious concern among circuit designers and architects. With decrease in cross-section area of copper interconnect resistivity increases due to surface roughness and grain boundary scattering, that causing increase in the propagation delay, power dissipation and electromigration. In ordered to understand the concept of increased resistivity, we look at the ITRS roadmap and some of the past works. From ITRS reports, we find that the copper resistivity for future technologies is increasing at a very fast rate as shown in Fig.1

In order to take the advantages that are achieved by scaling device dimensions, interconnect induced delay has to be minimized. The challenges of interconnect for nanometer scaling in VLSI devices have to be sought out through innovative futuristic design solutions, circuit & interconnect optimization techniques and material solutions, so that interconnects do not limit the benefits of continued device scaling. Thus in order to meet the demand and future requirement of interconnects Carbon Nanotube comes out to be most effective promising solution which has been recently proposed as a possible future replacement for metal interconnects in futuristic technologies.

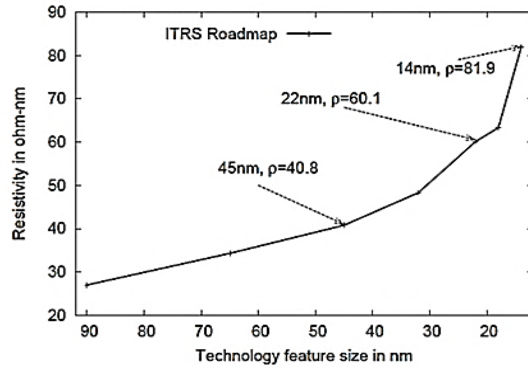

Fig.1 Resistivity increase as size decreases source from ITRS roadmap. There is a steep increase in resistivity as we move into 22nm and lower technology node (ITRS, 2007).

Table 1 gives us the highlights of the five most key challenges for the near term (≥22 nm) and long term (< 22 nm) as mentioned by ITRS. For the near term future, the most difficult challenge for interconnect is the introduction of new materials that meet the wire conductivity requirements and reduce its dielectric permittivity. And for long futuristic term, the impact of size effect on interconnect structures must be mitigated.

Table 1(a). Interconnect Difficult Challenges source from ITRS Roadmap (ITRS, 2007)

Difficult Challenges ≥ 22nm	**Summary of Issues**
Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
Engineering manufacturable interconnect structures, processes and new materials*	Integration complexity, CMP damage, resists poisoning, dielectric constant degradation. Lack of interconnect /packaging architecture design optimization tool
Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features; defect tolerant processes, elimination /reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.

Table 1(b). Interconnect Difficult Challenges source from ITRS Roadmap (ITRS,2007)

Difficult Challenges < 22nm	**Summary of Issues**
Mitigate impact of size effects in interconnect structures	Line and via side wall roughness, intersection of porous low-κ voids with sidewall ,barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
Three-dimensional control of interconnect features (with its associated metrology)is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at Nano-dimensions.
Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbates thermo mechanical effects. Novel/ active devices may be incorporated into the interconnect.
Identify solutions which address 3D structures and other packaging issues*	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

**Top three challenges*

CMP—chemical mechanical planarization *DRAM—dynamic random access memory*

3. Interconnect Modeling

The parametric analysis of copper and SWCNT bundle as interconnects for VLSI circuit is done in this section. Using these parameters, the performance of CNT bundle interconnects is compared to copper wires.

3.1 Modeling Parameter of Copper Interconnect (B P T M, 2010)

Resistance:-

$$r = \frac{\rho l}{wt} = \frac{(\rho_s + \rho_g)}{wt} l \tag{1}$$

where the resistivity ρ takes into account the effects due to surface scattering and grain boundary scattering. Expression for the resistivity is given by

$$\frac{\rho_s}{\rho_0} = 1 + \frac{3}{4}(1-p)\frac{l}{w} \tag{2}$$

$$\frac{\rho_g}{\rho_o} = 3[\frac{1}{3} - \frac{\alpha}{2} + \alpha 2 - \alpha 3ln(1 + \frac{1}{\alpha})] \tag{3}$$

Where

$$\alpha = \frac{l}{d} \times \frac{R}{1} - R$$

3.2 Modeling Parameter for SWCNT Interconnect

Resistance:-

An isolated CNT resistance comprises of mainly three components: (1) Fundamental resistance of 6:45k-Ω (2) Scattering resistance (3) Imperfect metal nanotube contact resistance. If the wire have mean free path less than 1 μm then its resistance is independent of wire length but if it have mean free path greater than 1 μm then it resistance increase with length due to scattering phenomena(A. G. Chiariello et al., 2009). Thus overall resistance of an isolated CNT wire (length > 1 μm) can be written as

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{\lambda} \tag{4}$$

Were λ is the mean free path, L is length of nanotube and $(h/(4e^2)) = R_F$ which is quantum resistance of bundle. If length < 1 μm, then resistance is given by quantum resistance (h/(4e^2) (Barry J. Cox et al, 2007). In actual practice, the observed resistance of a CNT is much higher than the resistance derived above. This is due to the fact that presence of imperfect metal-nanotube contacts which give rise to an additional contact resistance.

3.3 Modelling Parameter for SWCNT Bundle Interconnect

The number of SWCNTs in a bundle is given by(C. Thiruvenkatesan et al., 2009),(H.Aghababa et al., 2008)

$$n_{CNT} = nwnH - \frac{n_H}{2} \; if \; nH \; even \tag{5}$$

$$n_w n_H - \frac{n_H - 1}{2} \; if \; nH \; odd \tag{6}$$

were

$$n_w = \left\lceil \frac{w-d}{x} \right\rceil \tag{7}$$

$$n_H = \left[\frac{h-d}{\left(\frac{\sqrt{3}}{2}\right)x} \right] + 1 \tag{8}$$

where, nwis the number of "columns" in a bundle, nhis the number of "rows" in a bundle, and nCNTis the number of SWCNTs in a bundle.(SudeepPasricha et al., 2009)
Resistance:-

The resistance of a CNT bundle is simply the quantum resistance divided by n_{CNT}.

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \quad (9)$$

4. Comparative Analysis Of Interconnect Based On Parameters And Equivalents Circuit Described Previously

In this section, resistive parameter of Cu with Single Wall CNT are studied on the basis of parameters describe in above sections. For copper Berkeley Predictive Technology Model (BPTM)is used to study its

Parameters(B P T M ,2010).We measured and compare the resistance of copper interconnect with SWCNT interconnect and also study the impact of mean free path, width and length on the resistance that is measures by considering the geometries suggested in (N. Srivastava,2005) ,(H. Li et al.,2006) for 22nm.

4.1 Resistance Parasitic study with change in width of SWCNT bundle and Copper interconnect.

Since resistance of CNT bundle change with length as well as with mean free path thus we plot graph of CNT bundle with change in width and mean free path. With increase in width of interconnect number of rows used in CNT bundle increases from equation 7 and hence number of rows used is CNT bundle increases from equation 5. Rbundle inversely proportional to the nCNT from equation 9 and hence from Fig.1, with increase in width of interconnect resistance of CNT bundle decreases.

Table 2. SWCNT bundle resistances with change in width for different mean free path of interconnect.

Width(nm)	MFP(0.6 µm)	MFP(1 µm)	MFP(1.6 µm)
22	6895.44	4137.26	2585.79
32	3183.9	1910.37	1193.98
48	1391.6	834.96	521.85
64	776.33	465.8	291.12
90	389.79	233.87	146.17

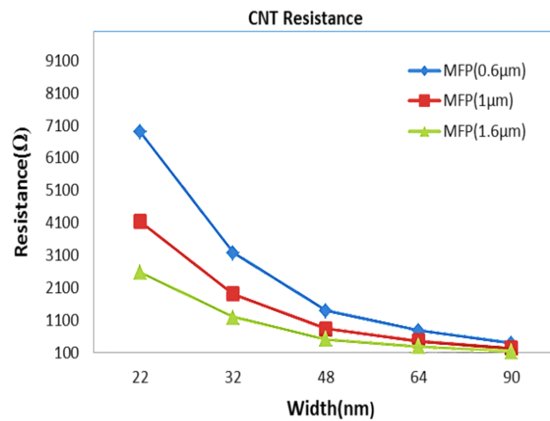

Fig.2 CNT bundle resistance verses width of interconnect for different mean free path at 22nm technology.

Table 3. Copper resistance vs. width of interconnect

Width(µm)	Resistance(Ω)
22	16666.6
32	7161.4
48	3182.87
64	1790.36
90	905.3

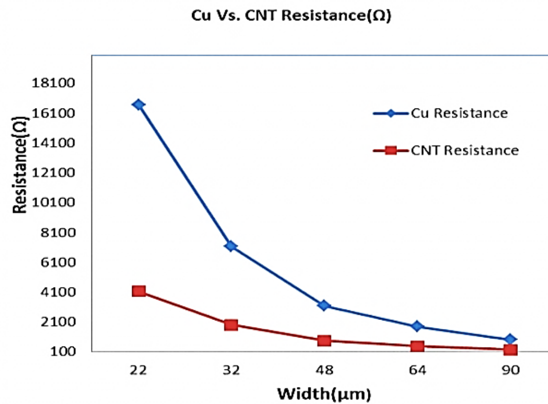

Fig.3 CNT bundle resistance (MFP=1 µm) Vs. Copper resistance with increase in width

For comparison of resistance of copper with CNT bundle we are taking the resistance of CNT bundle having mean free path 1 µm for simplicity.

From Fig.2 we observe that resistance of CNT bundle is less as compared to the resistance of copper with increase in the width of interconnect. Hence CNT bundle outperforms the copper in terms of resistance.

4.2 Resistance Parasitic study with change in length of SWCNT bundle and Copper interconnect

CNT bundle resistance depends on length as well as on mean free path from equation 4. Hence with increase in length resistance increases and thus Rbundle also increases from equation 9. Thus in Fig.3 resistance is increases with increase in length for different mean free path.

Table 4. CNT bundle resistance with change in length for different mean free path of interconnect

Length(µm)	MFP(0.6µm)	MFP(1µm)	MFP(1.6µm)
100	318.39Ω	191 Ω	119 Ω
300	954 Ω	573 Ω	357 Ω
500	1590 Ω	955 Ω	595 Ω
700	2226 Ω	1337 Ω	833 Ω
1000	3180 Ω	1910 Ω	1190 Ω

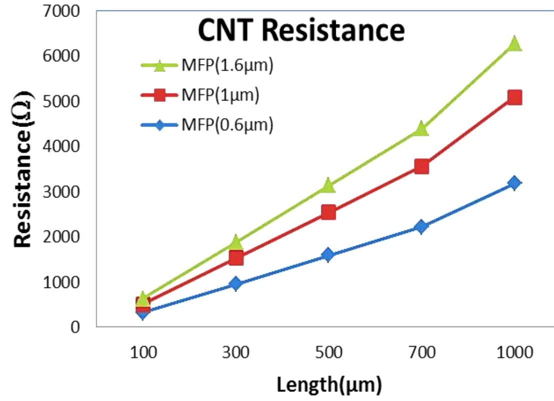

Fig. 4 CNT bundle resistance Vs. length of interconnect for different mean free path at 22nm technology.

Table 5. Copper resistance Vs. length of interconnect

Length(μm)	Resistance(Ω)
100	716.14
300	2148.43
500	3580.729
700	5013.02
1000	7161.458

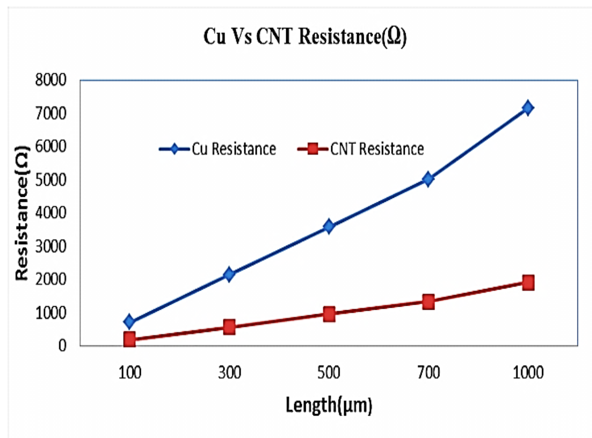

Fig.5 CNT bundle resistance (MFP=1 μm) Vs. Copper resistance with increase in length

Again for comparison of resistance of copper with SWCNT bundle we are taking the resistance of SWCNT bundle having mean free path 1 μm.

From Fig.4 we observe that resistance of CNT bundle increases less as compared to the resistance of copper with increase in the width of interconnect.

5. Conclusions

In this paper we have compare the resistance of SWCNT interconnect configuration with copper interconnect for different length and width. From analysis we have found that the SWCNT bundles have less resistance as compared to Cu. Thus by analysis of graphs we observed that the resistance of SWCNT bundle interconnect decreases with increase in width and is less as compared to copper which also decreases with increase in width. Also we observe that SWCNT bundle interconnect outperforms the Cu interconnects performance in terms of resistance with increase in interconnect lengths. Thus we can say that to overcome from the limitation of copper, Carbon Nanotubes have a great potential and a possible replacement of copper interconnect in future.

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